Final report

Project title	Multi-level medium voltage converter
Project identification (program abbrev. and file)	64014-0137 :Multi-level medium voltage converter
Name of the programme which has funded the project	EUDP
Project managing company/institution (name and address)	PowerCon A/S, Fabriksvej 6, 9560 Hadsund
Project partners	KK Wind solution, Aalborg university (AAU), PowerCon Embedded, PowerCon.
CVR (central business register)	DK32270433
Date for submission	30.06.2017

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1.2 Short description of project objective and results

The project "Multi-level medium voltage" converter is a development and demonstration project, which by proposing at new design aims at optimizing one of the most important subsystems in a wind turbine. It is a collaboration between research and industry companies and will boost creation of both engineering and production jobs in the sector.
The project succeeded by developing a new Converter system that reaches the targets in terms of efficiency and cost, by achieving a medium voltage system with the same cost as a low voltage design. The project demonstrated scalability with a kW demonstrator and efficiency and cost with a full scale 6MW version.

Projektet "Multi-level medium-spændingskonverter" er et udviklings-og demonstrationsprojekt, som ved at foreslå et nyt konverter-design har til formål at optimere en af de vigtigste delsystemer i en vindmølle. Projektet er et samarbejde mellem forskning og industri og vil øge skabelsen af både udviklings- og produktionsjob i sektoren.
Projektet lykkedes ved at udvikle et nyt converter system, der opnåede målsætningerne med hensyn til effektivitet og omkostninger ved tilblivelsen af et mellemspændings system med samme pris som et lavspændingsdesign. Projektet påviste skalerbarhed med en kW demonstrator samt effektivitet og omkostningsmål med en fuldskala demonstrator på 6MW.

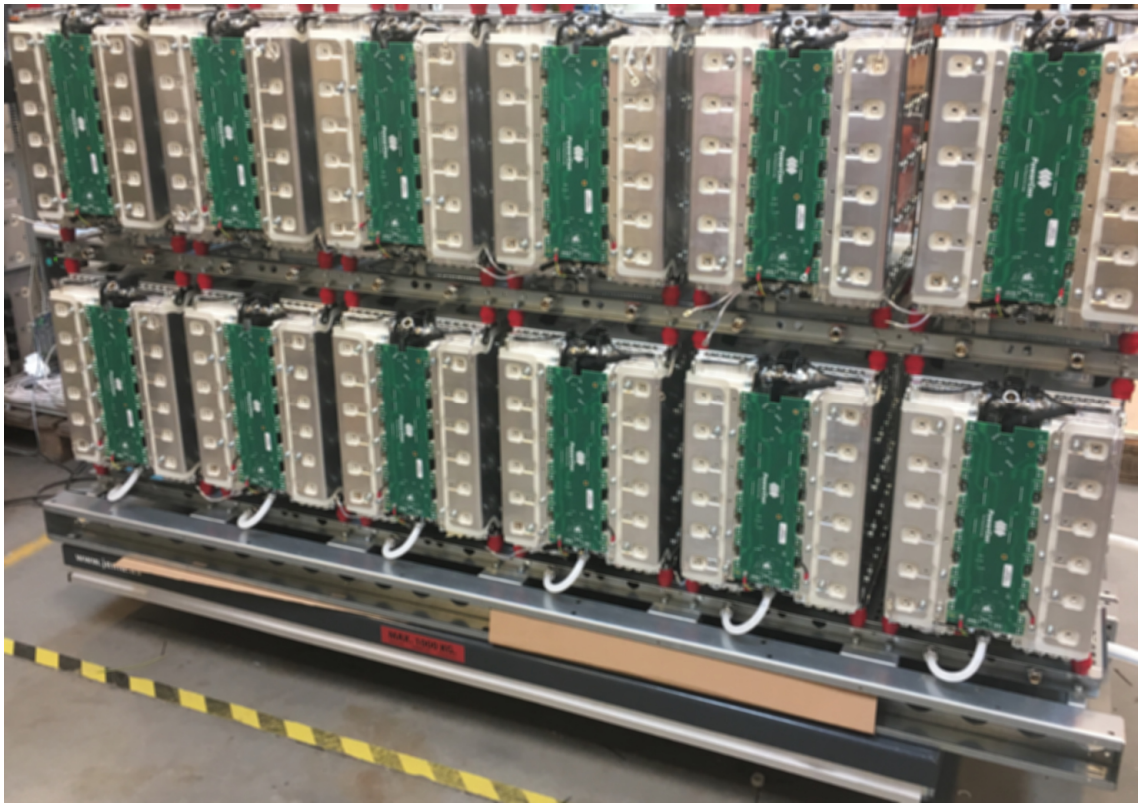
1.3 Executive summary

Cost efficiency gains are considered necessary to maintain public and political support for largescale implementation of offshore wind in Europe and globally, and to maintain the competitive edge of Danish actors in this market. A critical component in a wind turbine (WTG) is the power converter, which basic function in a wind turbine is converting a varying voltage/frequency from the generator into a fixed voltage/ frequency output synchronised to the power grid. The power converter is one of the most expensive subsystems after the blades and the tower, and one of the subsystems where the largest savings from a more cost-effective design are expected. As WTG's become larger, the power converter also increases in sizes causing an increased focus on the size, weight, efficiency, reliability and price. The price of the power converters for the current market is on one side depending on their physical size, the choice of components and the related design margin.

The most common type is the low voltage converter, and increasing turbine power has been accompanied by adding more low voltage systems in parallel. However, there is a pull from many of the WTG manufactures for the introduction of medium voltage (MV) converters. The pull is generated from the most powerful WTGs from 5MW and up, where the generators typical are MV, but also from the desire to have the converter down-tower for easier maintenance. The MV components are generally more expensive than low voltage components triggering the objective of the project to build a MV converter based on the less expensive low voltage converters. By stacking of low voltage system in series rather than parallel, a MV converter can be build using LV components. Thus, the proposed multi-level medium voltage converter system will bring the benefits from both systems.

The project succeeded in building a small-scale (kW) functional prototype for test of functionality at reduced power scale validating the control and communication system with a high number of levels in the system. Furthermore, the project also succeeded in building a 6MW prototype in full scale for demonstrating the full-scale

functionality, cooling methodologies and the cost targets of the system. In parallel with the construction of the two prototypes, production consideration and preparation were conducted and especially the PCB production has been evaluated, review and revised multiple times preparing for large scale production of the systems.



The positive results in relation to the achieved cost and functionality of the system has been acknowledged very well among potential customers. Because of this positive feedback there is a high expectation between PowerCon and KK in relation to the commercial future of the project.

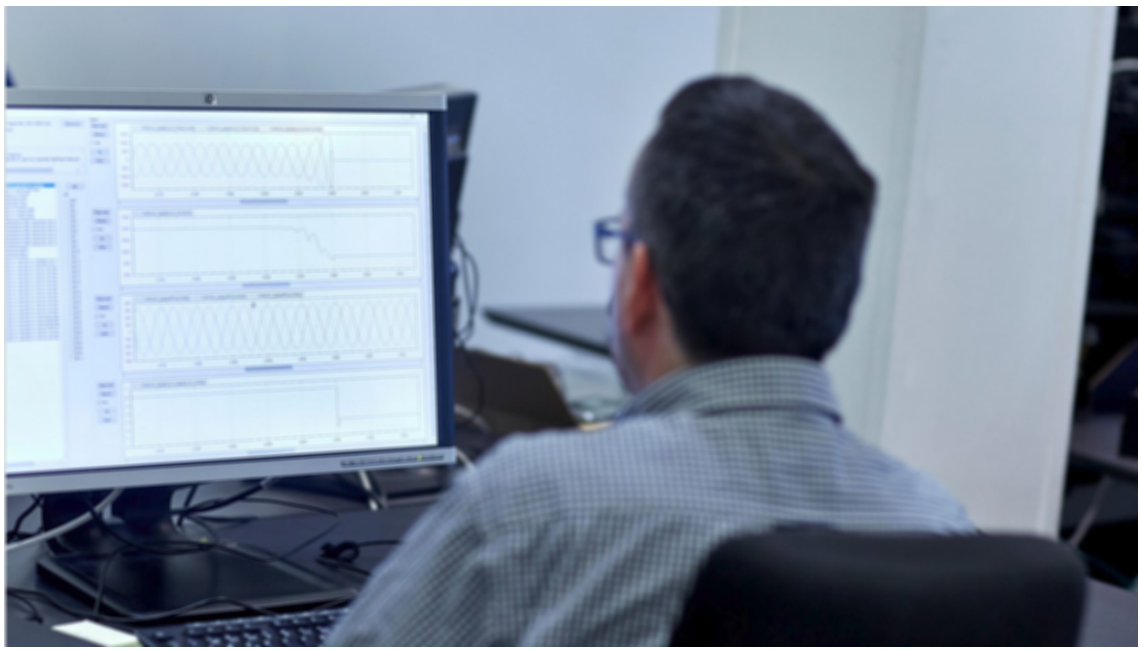
1.4 Project objektives

The overall project objective was to develop and demonstrate a new converter system enabling KK Wind solution and PowerCon to supply the system to customers within the wind turbine industry after the completion of the project.

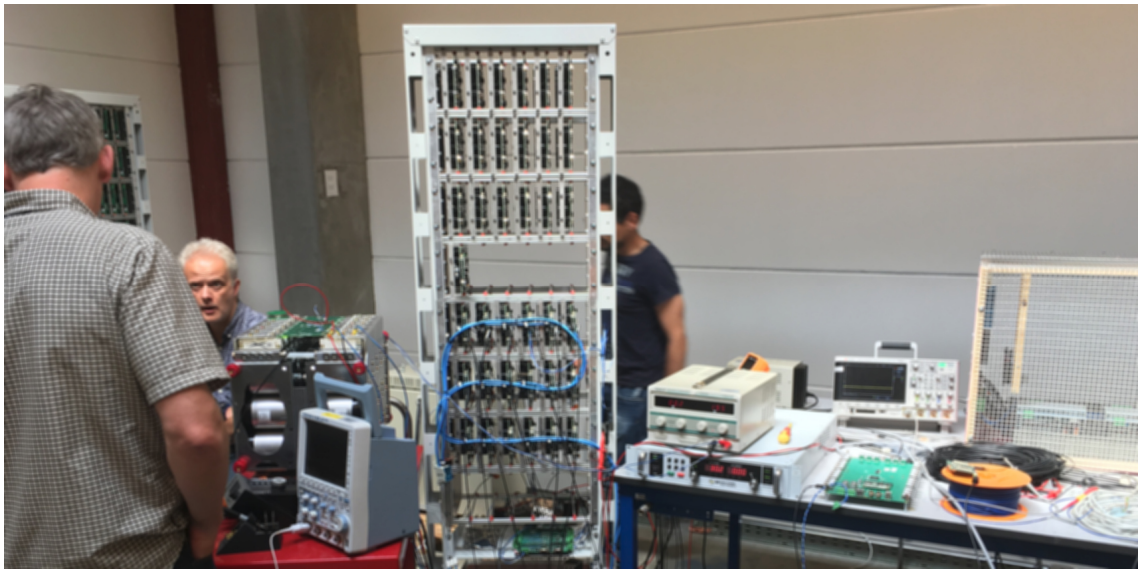
Technical objectives: The project had the goal to develop, produce and demonstrate the system in a version that can both visualize scalability compared to power production, and demonstrate the robustness of the system. Furthermore, the megawatt prototype should be close enough physical to visualize how the final solution would look like in a turbine.

Commercial objective: The commercial project partners will market, sell and produce the product after the technical objectives has been achieved. After the prototype developments and tests have successfully completed, the goal was to have a commercial agreement with a third-party end-user for field test of the system after the demonstration project.

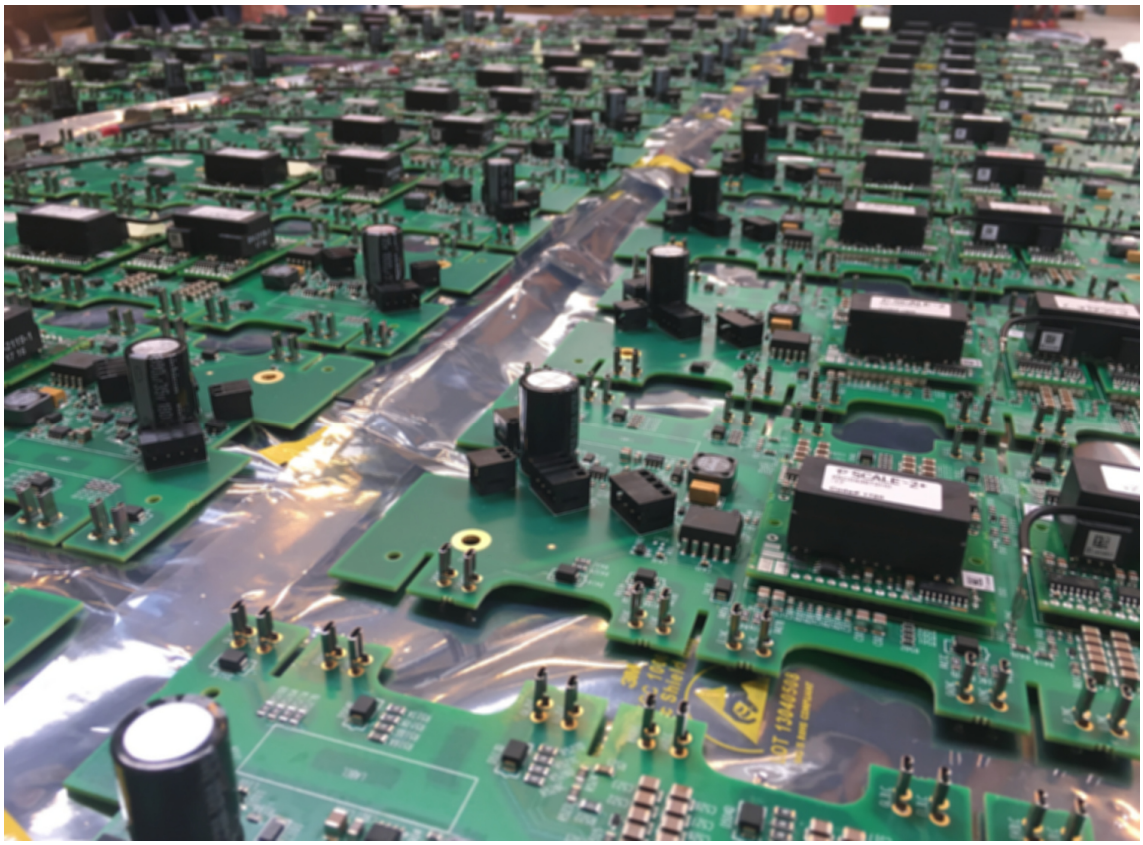
The project implementation started with Work packed 1, State of the art description and project requirement specification. This were done to ensure that the specified requirements meet the correct turbine and grid requirements and that the chosen technology was the optimum choice for the chosen application and the chosen solution could meet the project requirements. Based on the information gained in WP1, the development and demonstration of the small-scale kilowatt demonstrator was conducted.



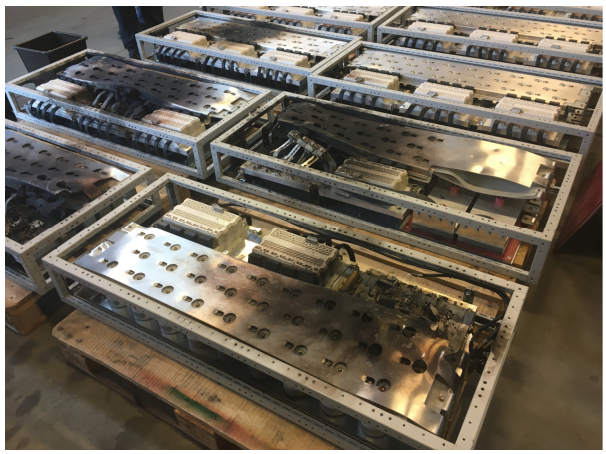
This was done to validate the controls and software design and thereby have the possibility of testing before developing the full-scale megawatt system. Development of the kW system was done while ensuring that the chosen design size and functionality were scalable with the final MW solution. In parallel with the kW design the megawatt development and demonstration was initiated with the WP3.



The design of the MW system includes design of the controller hardware and ensure that the chosen MW design was according to the requirement specification. Building the MW system also included extensive dialogs with component sub suppliers to select and validate the right components for the system. These tasks were also linked to WP4, ensuring the develop solution is optimized for state of the art production and relevant production requirements are fulfilled in the design. Especially related to PCB production since the multilevel design requires relatively large numbers of PCB´s for the distributed control.

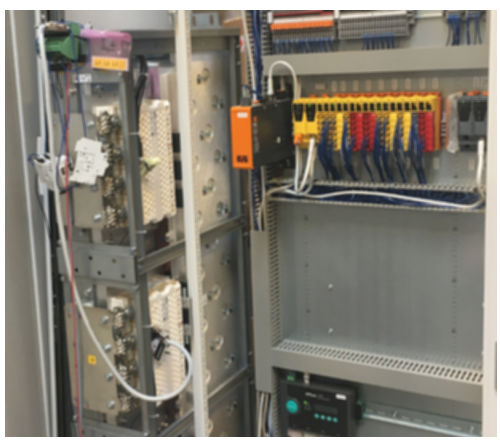


A central part of WP3 and WP5 was also to design and construct various test arrangements for the verification of submodules and the test of the complete system. For this purpose, more than 10 different test setups have been established with the aim of testing subsystems and components also well beyond their limits to evaluate failure modes and design ways of avoiding total system destruction.



Especially power modules (IGBT´s), capacitors and dump load resistors has been in focus when testing. These components are the most critical items in the system and some of the most expensive.

Because of this the project has tested different suppliers and different models to benchmark the quality and overall performance. As an example, capacitors from 4 different suppliers have been tested.



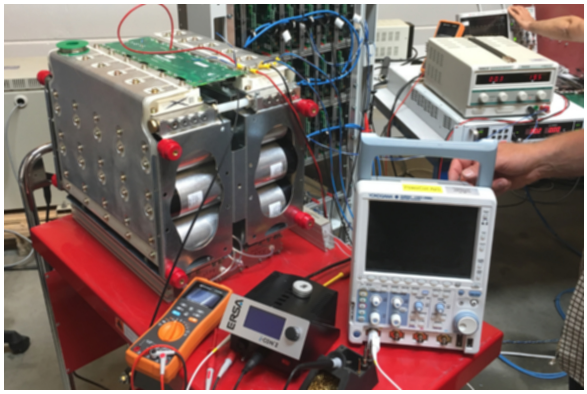
1.4.1 Project Progress

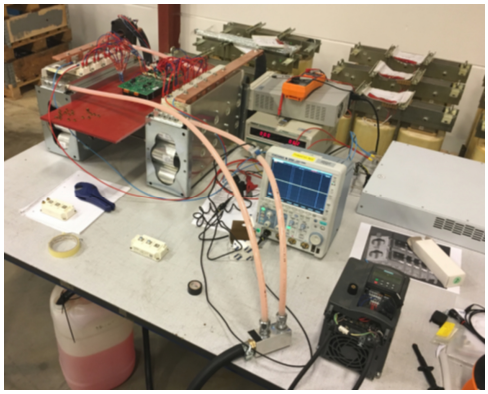
The project evolved slowly in the first months were most of the specification work was done. In this explorative phase, most of the partners were focused on including all possible requirements and afterwards cut down to the most relevant for the final Wind turbine application. In the first part of the project the partners also hired additional people to support the progress of the project. After WP1, the work with WP2, WP3 and WP4 were initiated. In these work packages, all the initial effort was oriented around software and control trying to cover all the specified requirements for the final system. These tasks evolved into very extensive workloads especially in relation to FPGA programming and despite that both the University and PowerCon Embedded hired additional FPGA resources the development time expanded the initial estimated hours. The outcome of the development was very promising and included functionality more innovative than original anticipated but the required development time postponed some of the following activities especially related to hardware design.

The development of the kW demonstrator hardware started with a limited number of prototypes to evaluate if the selected size and design was appropriate for accommodating the test functionality. This became an iterative process were modifications were made including new prototypes 3-4 times before the final design was produced in lager number corresponding to a total of 300 cells. The positive effect of these kW iterations was increase design confidence at a relatively low hardware cost, but the negative effect was a postponed construction of the more expensive MW system.

On the commercial side, the technical results gained from the demonstrators started the dialogs with potential customers and possible field test end-users. Important factor, besides the technical features, related to these discussing's was the cost of the system that strongly depended of the component cost. In relation to commercial agreements with component suppliers this task evolved to be quite important and significant in terms of use of resources since the project decided to evaluate and test different models, and brands of selected components to bench mark them and find the optimum in terms of performance and price.

After the selection of components for the MW demonstrator was completed the purchase was conducted. In generally the wind turbine industry has been blessed with increasing demands for turbines over the last years which in general is very positive for the project. However, in relation to component lead-times the increased demand increased the delivery times of components causing a delay in the MW demonstrator assembly. Worst case was the DC link capacitors going from a typical lead-time of 8 weeks to 22 weeks doing 2016.
To mitigate this delay, the decision was made to start the MW test on a few submodules instead, were the project succeeded in getting a limited number of components for.





Once the components for the 6MW demonstrator finally arrived the assembly of the MW system went very well without significant surprises.

1.4.2 Risks associated with the project.

Relating to risks in the project the initial anticipated risks were:

Risks	Risk level	Mitigation/Contingency plans
Technological risk in the design and the expected performance of the proposed system	Low	Modular multilevel converter concepts were applied successfully in industry for high voltage direct current (HVDC) transmission lines and flexible AC transmission systems. For medium voltage, it is just a matter of time before this technology enters the market, concepts being already proposed for machine drive applications
The expected cost saving of the design compared to current MV Converters	Low/Medium	The proposed system will be built on standard components. However, the size and price of the dc-link capacitors can be a bottleneck in the project. The type, number size of capacitors will be considered to minimize the additional cost compared with a low voltage system. Compared with MV systems the cost of additional DC-capacitors is not an issue since the MV systems is a lot more expensive.
Access to the market and commercial exploitation of the technology post-project.	Medium	Entering the market with a new generation of supplier of such a critical subsystem will be a challenge. However, both industrial partners have great economical interest in the idea and the technology post-project and KK already has a strong foothold in the segment.
Other suppliers (competitors) applies the same technology solution for their products.	Medium	One of the main purposes of this project is to get one step ahead of competition. Steps towards fast market introduction will be taken within the project by setting up field test agreements with third parties.

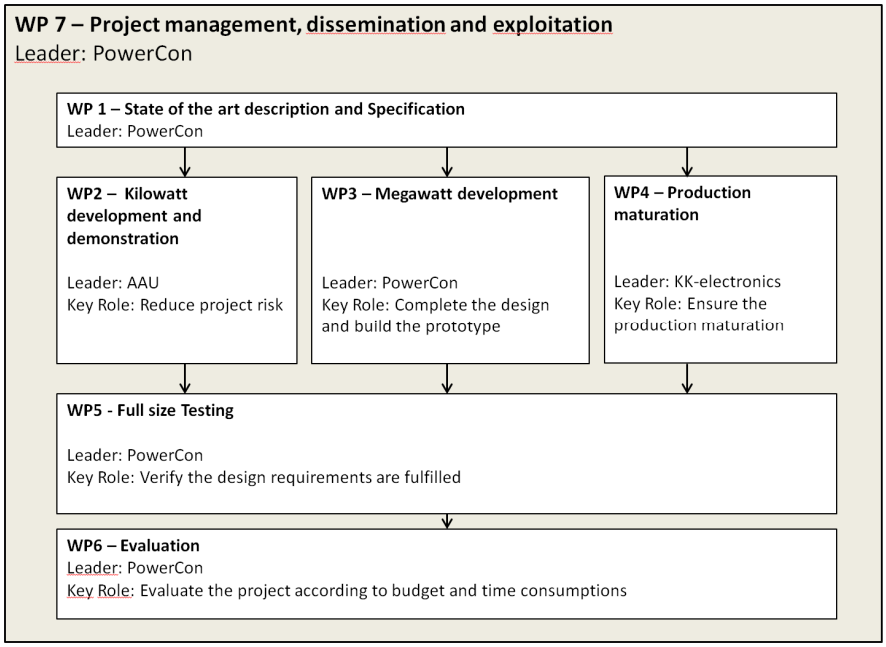
The technological risk in the design and the expected performance of the system has been reduced since the project succeeded and has lived up to the expectations. Also, the cost of the system and more precise the cost of the capacitors has turned out to the positive side because of the project achievements especially because of the effort put into test and comparison of various suppliers.
The last two commercial risks are still valid and will be addressed by a close follow-up with potential customers in the future. The risk that competitors will try to adapt the same technology is partly addressed by the project patent.

The overall project implementation and most of the milestones were achieved within the project timeline. Besides normal challenges with time consumption for development tasks the three-year project implementation went as planned. The last Commercial millstone (agreement with field test customer) for the partners to carry on with the commercialization after the project did however not succeed within the timeline. The project has had dialogs with more than one potential field test customer, and still have, but so far, no agreement has been made. One of the main reason is that the system is a vital part of the Wind turbine and customers argue that they need exclusive rights if they were to engage in the test of the system. The partners in the project are optimistic about these challenges and see it as a positive indication of the importance and value of the achieved results.

In general, no major issues or problems occurred in the project. Within the three years' time several minor challenges arise but most of them were mitigated with weekly project management adjustments. One of the most critical issues within the project were the expanded lead time of components from 8-22 weeks for the megawatt demonstrator components. In the end, the delay was absorbed within the project timeline but it was not expected to be an issue when the project was initiated.

1.5 Project results and dissemination of results

The main activities within the project was separated into seven work packages.



The technical results achieved has been related to these work packages and are summarized:

WP1, State of the art description and project requirement specification: Requirement specification, State of the art description, D-FMEA. All these were the foundation of the design and in the end the final product.

WP2, Kilowatt development and demonstration: kW system specification, Design and build the system, Validate control and software. The tasks related to the kW demonstrator that were designed, build and used for validation of the software and control.

WP3, Megawatt development and demonstration: Design og electrical hardware and cooling system, Develop the control and software, build the megawatt prototype. Designing and building the system also included the design and construction of several test benches to choose the correct components.

WP4, Production maturation: Production workflow, Production requirements and total system cost. These tasks and results have been both technical and commercial since the production activities are closely related to the cost of the system.

WP5, Full size test: Ensure the developed solution is according to the specifications, obtain experience with normal operation and induce faults to verify system safe operation. Testing activities have been a very big part of the project and have provided many results both for the development process but also for the commercial engagement with potential customers and on the other side input for the component supplier selection.

WP6, Evaluation: Evaluate the project results according to the expected goals and leanings for future projects. This is accomplished and the evaluation among the partners are very positive in relation to the overall result of achieving a MMC systems that complies with the requirements from WP1.

WP7, Project management, dissemination and exploitation: The project execution has been achieved and the results are very satisfying for the project partners. In terms of the dissemination a plan was made and communicated to the partners and agreed upon. The main targets for the companies in the project are potential customers were meetings and dialogs will be continued after the project. KK and PC have agreed on ways to exploit the project soon, including joint marketing activities to promote the system.

The technical objectives of the project have been achieved. These were to develop, produce and demonstrate the system in a version that can both visualize scalability compared to power production, and demonstrate the robustness of the system. Furthermore, the megawatt prototype should be close enough physical to visualize how the final solution would look like in a turbine. The expectations in relation to the performance end efficiency has also been tested, which conforms very well with the expected and equal to more than 0,5% efficiency gain on turbine level. Besides achieving the expected results some additional positive results have been obtained in terms of weight and size, of the system. These factors are important for the wind turbine integration and compared with the electrical power this determine the power density of the system. The achieved results are, approx. 0,8 ton/MW and 1.2 m3/MW, two numbers that are very positive compared with other converter systems. Below are the preliminary Data sheet:

Technical Characteristics
Medium Voltage Multi-Megawatt
PC - MMC - Wind

PowerCon

General Data	Modular Multilevel Converter (MMC)
• Rated power range	6 - 60MW
• Converter type	Back to Back – MMC (DC split on request)
• Semiconductor type	IGBT
• Efficiency (at rated power)	>98.3%
• Generator type	IG / PMG / SG
• Product certification	CE (UL, CSA… on request)
• Application	Onshore / Offshore
Electrical data	
• Rated AC output voltage range	3.3 – 33kV
• Rated DC output voltage range	5 – 50kV
• Grid voltage range	-10% to +10%
• Nominal frequency range	5-150Hz
Grid filter	
• Power Converter THDi	<5% (other values on request)
Generator filter	
• dV/dt	1.5 kV/µs (other values on request)
LVRT	
• LVRT/FRT compliance	Symmetrical and asymmetrical voltage faults down to 0 % residual voltage, and up to rated reactive current support. Complies with the strictest grid codes, such as SDLWindV 2009, NERC PRC-024-1 or GB/T 19963-2011.
Cooling	
• Type	Water/Glycol cooled (Liquid)
• Inlet temperature range	0°C to +55°C
Mechanical data	
• Protection degree (IP)	IP54 (higher on request)
• Corrosion class	C3 - High (higher on request)
• Mass	Approx. 0,8 ton/MW
• Volume	Approx. 1.2 m^3/MW
Communication	
• Protocols	All industry standards supported
Ambient conditions	-40°C to +40°C

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Regarding the commercial objectives most of these has also been realized. The commercial project partners have agreed to market, sell and produce the product once the first customer is signed. The partners are very optimistic on this based on the technical achievements and especially the realized system cost. The the goal to

have a commercial agreement with a third-party end-user for field test of the system after the demonstration project were however not accomplished within the project period. As mentioned above, the project has had dialogs with more than one potential field test customer, and still have, but so far, no agreement has been made. One of the main reason is that the system is a vital part of the Wind turbine and customers argue that they need exclusive rights if they were to engage in the test of the system. The partners in the project are optimistic about these challenges and see it as a positive indication of the importance and value of the achieved results.

Besides the positive dialogs with potential customers concerning using the product in wind turbines, ongoing ideas concerning the use of the technology for varies test are have also been very positive for the project partners. This has not yet lead to any direct turnover but several projects are being discussed and some of them with the aim of installation outside Europe. Within the project period the partners have hired additional engineers to assist with the development of the system. This is expected to continue in the coming years and technicians to work in the production of these systems are expected to be increased. Assuming the first wind turbine customer will require 100 systems per year, this would be equivalent to 25 people in the production + additional engineers etc. to support the production and the product.

The general dissemination of the results has primarily been in the form of student papers at the University, customer meetings and attending fairs.

1.6 Utilization of project results

The project participants are both companies and a university. The university expect to use the results for future student studies and to provide a platform that can easily be used for students and projects. The companies expect to market and sell products originating from this projects results.

The project has established a dissemination plan to identify and organise the activities to be performed and promote the commercial exploitation of the project's results and the dissemination of knowledge from the project. The plan includes marketing activities to enhance the commercial potential of the system and at the intention of the notification of projects results in the scientific sector represented by the University of Aalborg. Dissemination concentrates on disseminating the results of the project itself to a wide range of existing and potential stakeholders. Special attention will also be paid to the transfer of knowledge to new students by means of future lectures at the university.

The main goal of dissemination plan is to create awareness of the project and the partners involved, present the projects achievements technical and commercial and to present the partners as trustworthy technology- and system providers. The objectives are to establish dialogs with possible customers and commercial partners and ensure the unique selling points are communicated in a way that potential customers can relate to them by converting project achievements into customer added values. It's also to communicate novel technical achievements, demonstrate the partners acquired skills and positioned the partners as leading within MMC technology. The target users are:

- Management (CEO/CTO/CFO), R&D engineers, purchase/sales departments, political persons and students within the field of power electronics

- Applications for medium- and high voltage AC-AC, AC-DC frequency converters in general
- Manufactures of Wind Turbines
- Test centres within various large scale electrical products and related grid connections
- Power distribution companies, HVDC and Statcom application
- Universities and other research institutes

To reach the target users the content is expected to be centred around technical achievements compared with current state of art, cost benefit analysis compared with present alternatives and business models for achieving the product or technology. This content is expected to be communicated through multiple sources such as; existing network, scientific papers, technical newspapers such as energy-supply etc. and fairs such as PCIM in Nuremberg. Also, direct marketing to known stakeholders, presentations, meetings, e-mails and online medias, company website, LinkedIn and the use of technical newspapers, articles/ papers/ publications and invitations for live system demonstration.

The dissemination activities have been successful if the project information reaches a wide range of relevant persons within potential customers and commercial partners. The success is also determined by the receiving parties understanding of the provided information and approval of unique benefits compared with current state of art.

The first version of a business plan is made and shared between KK and PowerCon. This includes the roles and activities expected to be addressed with the first customer and onwards. Future more expected impact on resources and facilities are addressed.

The business plan is built around supplying products to customers based on the MW demonstrator prototype that originate from this project.

The market potential is expanding compared with the expected size 3 years ago, primarily because of the increased power on onshore turbines. The recent announcement of close to 4MW power range from more than one of the leading manufactures is enabling the profitable use of MMC converters in onshore as well as offshore wind turbines. The increased power level will make it profitable for some of the onshore turbines to increase the voltage level and thereby gain some of the efficiency savings with the MMC technology compared with traditional converters.

For the protection of the technology, the first patent application is filled and more are likely to follow in near future.

1.6.1 Relevance for Energy-policy goals

As the wind turbines are growing in power output and moving offshore there is a pull from many of the turbine manufactures for the introduction of medium voltage (MV) converters. The pull is generated by the desire to have the converter down-tower for easier maintenance, as the energy loss in a design using MV converters distant from the generator is lower compared to low voltage converters. But also from the available generator types in 5MW+ wind turbines, which are typical becoming MV generators. Despite the tendency of MV converter solutions being more expensive, the increasing turbine power is forcing the manufactures to consider a voltage change instead of adding more low voltage systems in parallel. The

achieved results in form of the multi-level medium voltage converter system with the benefits from both systems, time wise fit perfectly into this dilemma.

The project results by developing, produce and demonstrate the system in a version that can both visualize scalability compared to power production, and also demonstrate the robustness of using the system.

This project will be contributing to the long-term objective to convert the Danish energy system to be 100 % based on renewable energy, of which the exploitation of wind energy has been a key driver. As wind is gradually becoming a source of energy considered on a par with energy sources, it is not only assessed based on its environment- friendly impacts, but also based on a Cost of Energy (CoE) consideration. The push for cost efficient alternatives to fossil fuels is driving innovation efforts in the wind energy industry, which is striving to improve the performance and reduce the costs of wind turbines (WTGs).

More specifically, one of the key policy and strategic references for this project is the Megavind partnership between the Danish Government and Wind Industry. As part of the main strategic objectives for wind power research, development and demonstration, the partnership recommends that the Danish public funds for research, development and demonstration of wind power are prioritised within a number of areas to support the existing research and strengthen research areas that are central to the industry. One is

"to develop wind turbine electrical design around the design of generators, power electronics, electric transformation and transformation as well as the control and regulation"

The conclusion is that there is great opportunity for development of new products and capabilities and in particular, the development of software for controlling the electrical system and the individual wind turbine has great commercial potential.

In Megavind's strategy for wind turbine components and subsystems, it is concluded turbine sub-systems hold greater potential for CoE reductions than others and some of the areas with most potential includes components in the electrical system. Emerging technologies pointed at are new multi-level converter concepts and the specific recommendation is at overall optimisation of the conversion system from generator to grid. By designing an optimised system with focus on the interaction between single components of the system, savings can be achieved for the complete system.

This project will strengthen Denmark's position in supplying innovative solutions to the ongoing work of delivering competitive wind energy. Only very few companies in Denmark has the skills and experience to competed international within the field of power electronics when it comes to development of wind turbine converters. Furthermore, the close collaboration with AAU, KK and PowerCon on this project is also very much aligned with the strategy of bringing universities and companies closer together, another recommendation of Megavind. The proposed project also strengthens PowerCon and KK-electronics in corporation as a system-integrating supplier, another important factor of keeping Denmark in front and lowering wind turbines COE.

1.7 Project conclusion and perspective

The project has succeeded in developing and demonstrating e new and very competitive converter solution.

The competitiveness is achieved by a combination of advanced technical features, a very robust design, improved efficiency and a very competitive price. Advanced technical features such as multilevel switching performance are creating new possibilities in relation to grid performance, a functionality that has gain more value as turbines are getting bigger and more dominant in the modern electrical grid. The robustness of the system combined with the modelized approach makes the system suitable for long service intervals and thereby a low level of operational costs.

Having achieved a system with less than 1,7% loss and the possibility of removing the high voltage transformer is also very competitive compared with present turbine converters, and in many cases an improvement of 30-40% looking at the converter alone. On turbine level, this corresponds to in the range of 0.5-1,5% efficiency gain, that alone is a very promising achievement. All these enhanced features are very positive and combined with a competitive system cost this is creating very positive chance of a wide market introduction.

The future perspectives of continued development relating to turbine systems and test equipment are already in the planning phase. Also new market possibilities such as Onshore Power Systems for the maritime market are in progress since the multilevel design also provides some interesting features towards supply and charging of electrical and hybrid ships.

Annex

- M. Ricco, L. Mathe and R. Teodorescu, "FPGA-based implementation of sorting networks in MMC applications," 2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), Karlsruhe, 2016, pp. 1-10.
- M. Ricco, L. Mathe and R. Teodorescu, "New MMC capacitor voltage balancing using sorting-less strategy in nearest level control," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8.

FPGA-based Implementation of Sorting Networks in MMC applications

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Acknowledgements

The paper has been supported by the EUDP through the grant number 64014-0137.

Keywords

«Multilevel Converters», «Converter Control», «Field Programmable Gate Array (FPGA)».

Abstract

In this paper an implementation technique for Field Programmable Gate Array (FPGA) devices of two Sorting Networks (SNs) used for control of Modular Multilevel Converter (MMC) is presented. In such applications, the classical sorting algorithms are based on repetitive/recursive loops, and they are usually implemented in microcontrollers or DSPs. However, they are not convenient for hardware implementation due to their inherent sequential operation. Instead, the proposed SNs, are suitable for FPGA devices thanks to their fixed parallel structure that allows improving the timing performance of the capacitor voltage balancing algorithm. The advantages and the main challenges of the Bitonic SN and Even-Odd SN in MMC applications are discussed. Moreover, in order to pre-evaluate the required resources and the execution time, equations are derived for both the proposed SNs and then a comparison is performed between them. The proposed equations are validated by comparing the real required resources with the estimated ones by using the Xilinx Vivado Design Suite tool. Finally, the operation of the proposed Bitonic SN is also tested in Vivado Simulator, achieving the sorted list of 8 elements in 18 clock cycles as expected.

Introduction

Nowadays, the Modular Multilevel Converter (MMC) has become a promising solution in both: high voltage direct current (HVDC) and high-power motor driver applications. Thanks to several advantages, such as high modularity, scalability, low harmonic output voltage content, low switching losses and high reliability, the interest in this topology has increased in both industry and academy [1]. However, MMC presents several challenges, like the necessity to control the circulating current, ensure the balance of the losses among the Sub-Modules (SMs) etc. An important objective is to maintain the Capacitor Voltages Balance (CVB) during operation, and one of the most common approaches is based on Sorting Algorithms (SAs) [2].

In MMC applications, the SAs are usually implemented in microcontrollers or in digital signal processors [3], [4]. However, Field Programmable Gate Array (FPGA) devices are more and more used due to the possibility to exploit the inherent parallelism of the algorithm to be implemented [5], [6]. Therefore, the CVB control, and then the sorting method, should be chosen in a way to obtain an optimal implementation for such a device. The implementation of SAs in FPGA is an important challenge mainly due to the timing performances of this kind of algorithms that could slow down the CVB [5]. Moreover, due to its inherent iterative statements, the pre-evaluation of the required resources becomes difficult. In literature these problems are overcome by implementing min/max methods which find the sub-modules with the maximum and the minimum capacitor voltage. For instance, in [6] the tortoise and the hare sorting method is implemented in FPGA. This method is particularly suitable for such a device thanks to its concurrent structure. However, in case of failure or

when the capacitors are approaching the maximum allowable voltage, more sub-modules must be inserted or by-passed during one sampling period. A solution is to run multiple times the max-min method which could lead to the same problem mentioned above, i.e. the controller response could slow down. For all these reasons, the aim of this paper is dealt with the implementation of sorting methods in FPGA device specialized for MMC requirements.

In other applications, such as data processing, sorting methods are implemented in FPGA by using Sorting Networks (SNs) [7], [8]. The SNs are well suited for hardware implementation due to their fixed parallel structure. Moreover, they do not require iterative (loop operation) or cascaded branches instructions (cascaded "if" instructions). To the best of the authors' knowledge, this is the first time that the SN FPGA-implementation for MMC applications is afforded. Three SNs are presented: Bubble SN, Odd-Even SN and Bitonic SN; and their peculiarities in MMC applications are shown. Some equations for evaluating their required resources and execution time are also derived and a comparison between the Bitonic SN and the Odd-Even SN is made.

The paper is divided as follows: firstly, a modular multilevel converter overview is given. Then, SNs are presented and their peculiar aspects in MMC applications are treated. The required resources and the execution time are estimated and compared with the real ones. Finally, conclusions are drawn.

Basic Operation of MMC

A schematic representation of a three phase grid connected MMC is shown in Fig. 1. It consists of an upper and a lower arm per phase-leg where each arm is composed by N series connected SMs, an arm inductor L_{arm} with its series resistance R_{arm} [9]. In literature different SM topologies can be found and one of the most commonly used is the half-bridge structure. According to the applied gate signal, this topology permits to insert the SM capacitor, by adding its capacitor voltage to the MMC arm voltage, or to bypass it, by inserting zero volts into the arm voltage [1].

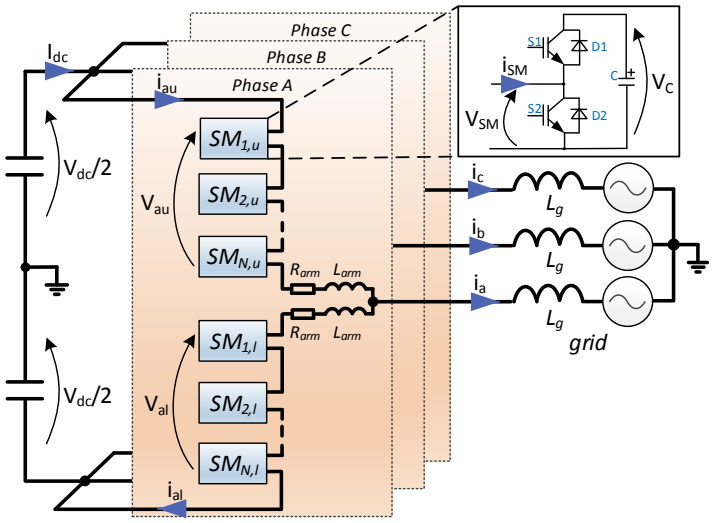
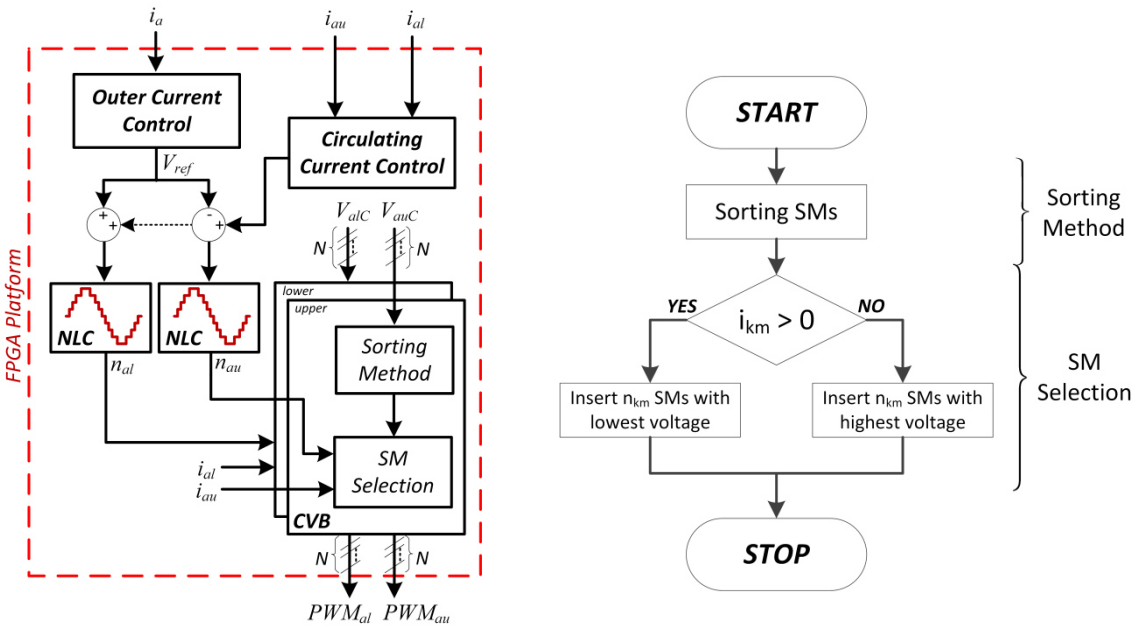


Fig. 1: Schematic representation of a grid connected MMC.

Different algorithms can be found in literature to generate the gate signals. However, each technique requires a proper CVB for reducing the voltage ripple component. Two kinds of CVB control were presented: the individual control approach, used for phase-shifted PWM, and the global arm control approach, adopted in the Nearest Level Control (NLC) [10]. The individual control approach is based on a closed loop control whose purpose is to keep the average capacitor voltage closes to a reference value [11]. Therefore, the modulation signal of each SM is adjusted, resulting in different references for the pulse generation. In this approach, the main issue is the tuning of controller parameters. An inappropriate tuning could affect the other control loops or leads to stability problems. The global arm control approach, instead, selects the suitable SMs for insertion/bypass according to the capacitor voltage and the arm current direction. In this case, no control loop is required, but a sorting based on the capacitor voltages is necessary.

According to this last approach, the MMC control scheme for the phase *a* is depicted in Fig. 2 (a). The outer current control loop calculates the reference voltage V_{ref} for each phase from the measured grid currents. The phase reference voltage is adjusted for the upper and lower arm in according with the circulating current control loop and the insertion indices n are then calculated using the NLC [12]. The achieved insertion indices for the upper and lower arm n_{ku} and n_{kl}, respectively, are sent to the corresponding CVB control module along with the measured capacitor voltages V_{kmC_i} and the arm current i_{km}, where *k* represents the phase (*k* = *a, b, c*) and *m* specifies the arm (*m* = *u, l*). The CVB consists of the sorting method and the SM selection block, which selects the proper SMs to be inserted and generates the corresponding gate signals. Beside the block diagram a flowchart of the basic CVB, executed in each sampling period, is shown in Fig. 2 (b). In order to reduce the number of switching, different methods were proposed in [13]–[16]. However, in this paper the focus is on the sorting method, which is the most challenging aspect of the CVB control implementation in a FPGA device. Indeed, the common SAs have limited timing performances [5] due to their inherent serial structure that makes them suitable for microcontroller or DSP implementation but inconvenient for FPGA devices. Moreover, due to their inherent iterative statements, the timing and resource evaluation in such a platform becomes difficult. For these reasons, the SNs are proposed for MMC applications and their implementation is discussed in the next sections.



(a) (b)

Fig. 2: (a) Block Diagram of the MMC FPGA-based controller for the phase a; (b) Basic flowchart of the CVB in NLC.

Description of the Sorting Networks

Sorting Networks are widely studied in literature [7]. They consist of a fixed parallel structure composed by m-horizontal wires and several Comparator-and-Swap (CS) operators. The latter can be drawn using the Knuth notation " ". This operator compares two unsorted elements: in case they are already sorted, it does not change anything; otherwise it swaps the position of the two elements. Fig. 3 shows three different 8-inputs sorting networks: Bubble SN, Even-Odd SN and Bitonic SN. They are composed by different stages which in turn are composed by several CS operators. The SN takes the unsorted list, noted with *x* on the left, and gives the sorted result *y* on the right. Each wire only takes one b-bit element.

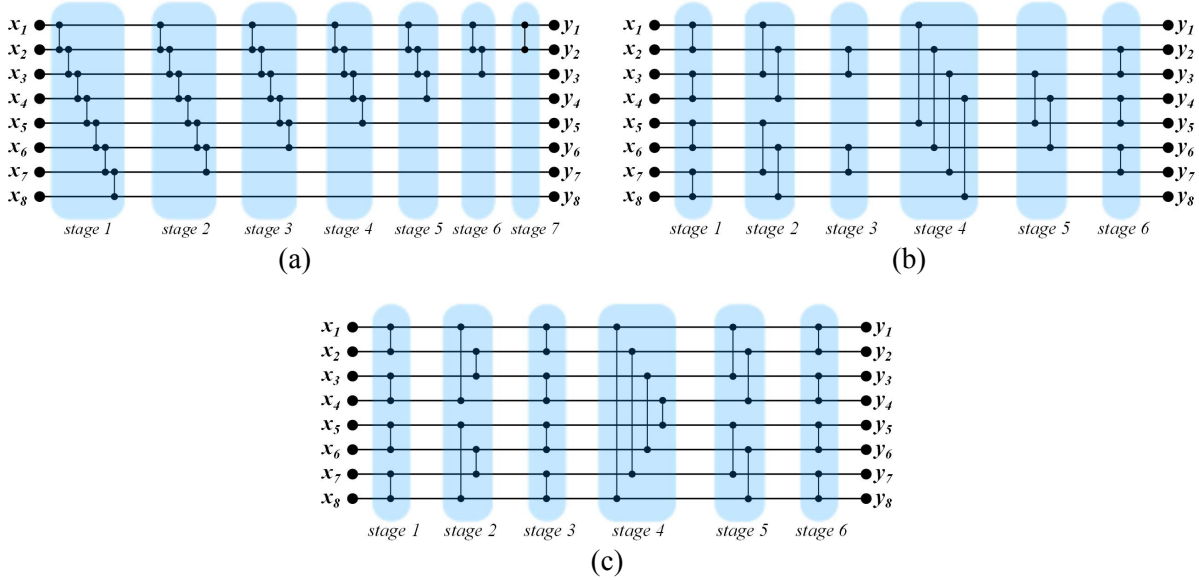


Fig. 3: Sorting Networks applied for a list with 8 inputs: (a) Bubble Sorting Network; (b) Even-Odd Sorting Network; (c) Bitonic Sorting Network.

As it can be seen in Fig. 3 the Bubble SN requires more stages and more CS operators in order to obtain the sorted list, while Even-Odd and Bitonic SNs give the results in fewer steps. It has to be noticed also that Even-Odd and Bitonic SNs provide the possibility of modularization of the network [7]. For these reasons in the paper the attention is focused on the Bitonic SN and on the Even-Odd SN.

Sorting Networks in MMC Application

Different peculiar aspects in MMC applications are now considered. Firstly, the SN element x_i has to be composed of the acquired capacitor voltage V_{kmC_i} and its corresponding physical position P_{kmi} of the SM in the arm. In Fig. 4 a 4-inputs Bitonic SN is presented as an example. The voltages are compared, and if they are not in the right order both the voltages and their positions are swapped (as the first CS in the first stage of Fig. 4). The output of the SN is the list y which has the voltages in decreasing order with the corresponding physical SM position. Therefore, if it is needed to insert or bypass the SM with the highest voltage, the first element y_1 has to be selected; otherwise the last one y_4 is considered.

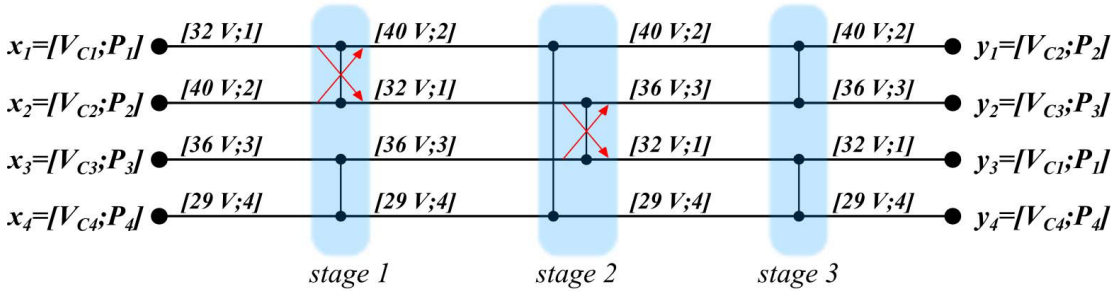


Fig. 4: Example of a 4 SMs MMC where Bitonic SN is used to obtain the ranked list based on the SM capacitor voltages for a generic arm.

Another aspect is related to the length of the list. Indeed, one of the main advantages of the MMC consists in its modularity [2], namely the possibility to increase the power rating by adding more modules in the arm. This implicates that the length of the list to be sorted is not known a priori. However, it is always possible to assume a maximum possible number of SMs in an arm (named here with M) and then the SN has to be developed for this worst case scenario. In these conditions the actual length of the list N (number of SMs) can be different from M (number of inputs in the SN, it must be a power of 2) and then some elements will be left empty. For ensuring the right behavior of the SN, these dummy elements have to be filled. A good choice should be set the voltages equal to 0

and the position to an unreal value (for example $P = -1$). In this way these elements will be kept in the last positions and when the SM with the lowest voltage is required, the last element with a position different from *-1* will be selected.

Fig. 5 shows an example of an 8-inputs Bitonic SN when the MMC is composed by 3 SMs per arm ($M = 8$ and $N = 3$). If the SN is modular, as in the Bitonic and Even-Odd SNs, it will be possible to achieve the result before the last stage by considering only a part of the network, as shown in Fig. 5.

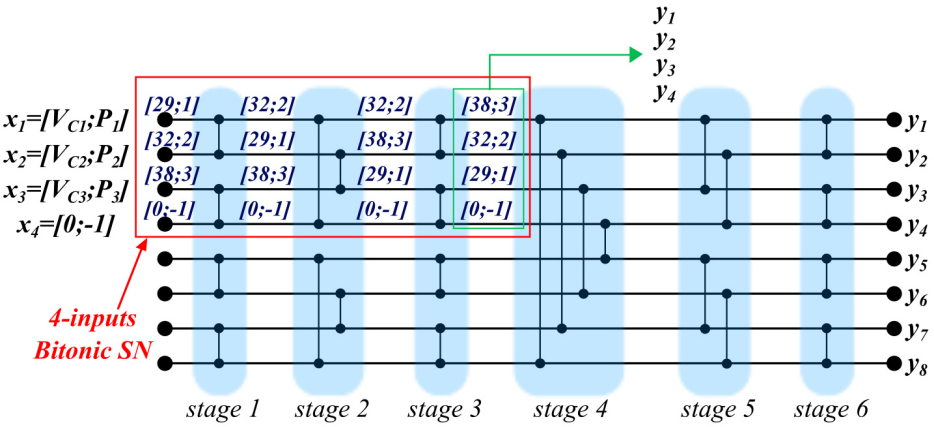


Fig. 5: Example of 8-inputs Bitonic SN when the length of the sorting list is equal to 3. The SN can be modularized.

After having discussed the main peculiar aspects of SNs in MMC applications, the evaluation of the FPGA resources and the execution time is afforded in the next section.

Resource and Time Evaluation for the FPGA implementation

First of all, the required resources for the CS operator have to be evaluated. This element is identical for all the networks and it consists of a comparator and 4 multiplexers, as shown in Fig. 6 (a). First the capacitor voltages are compared and then the multiplexers select the maximum and the minimum capacitor voltages along with their corresponding physical position. Therefore, if V_b is larger than V_a, the comparator output will be 1 and then the multiplexers will swap the voltages and the positions by selecting their second inputs. If V_b is smaller than V_a, the comparator output will be 0 and then the multiplexers will select the first inputs by avoiding the swap operation.

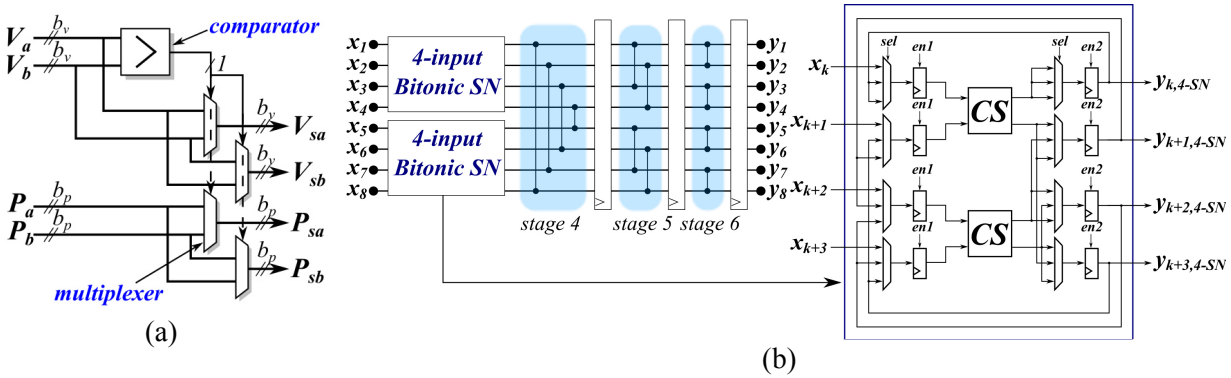


Fig. 6: (a) Comparator & Swap FPGA Implementation; (b) Factorized Fully Pipelined Synchronous 8-input Bitonic SN with factorization level equal to 4.

In [7] the resource evaluation for a classical CS operator, i.e. without the position value, is accomplished. The authors of [7] showed that for implementing the comparator and the 2 multiplexers, $\frac{5}{2}$ b LUTs are necessary (considering 5-input LUTs as in Virtex 5 FPGA devices), where b is the bit length of the input elements. In case of MMCs, in addition to the classical CS structure, 2

multiplexers for selecting the position are required and then the number of LUTs for implementing the proposed CS operator becomes:

$$LUT_{cs} = \frac{5}{2} b_v + 2 b_p \tag{1}$$

where b_v and b_p are the bit lengths of the capacitor voltage and of the position value, respectively. It is worth to note that this is the minimum number of LUTs required for implementing a CS operator. It corresponds to an optimal packaging with maximum density, namely all the LUT inputs are used. The placer could not use this maximum packing strategy for optimizing other aspects, such as the routing distance. However, during this resource evaluation, this optical packaging is considered in order to compare different SNs.

In the following, fully pipelined synchronous sorting networks are considered for increasing the maximum clock frequency of the architecture. This kind of architecture is driven by an external clock signal that synchronizes the data through the SN. After each stage a bank of flip-flops is allocated for storing the results of CS operators during the rise-edge of the clock signal. Therefore, a new list can be fed to the input of the SN every clock cycle.

In [7], being a data processing application, the implemented SN has to treat the input signal continuously. Therefore, one of the objectives was to increase the throughput of the architecture by adopting the fully pipelined synchronous SN and by sending new input set at each clock period. In MMC applications, instead, the treatment is synchronized with the NLC controller and then the sorting of 6 lists (that correspond to 6 arms of a three-phase MMC) is accomplished at each sampling period. For this reason and for reducing the required resources, some CS operators can be reused. This will increase the execution time but it will strongly reduce the required resources.

The idea presented in this paper is to share the CS operators contained in a sub-module of the SN. Therefore, it needs to choose the length of the input list *M* and the factorization level *L*, namely which SN sub-modules have to be factorized. Fig. 6(b) shows an example with *M = 8* and the factorization level *L* equal to 4. This means that the sub-modules 4-input Bitonic SN will be factorized.

This solution allows reducing the required CS operators and then the required resources. Indeed, the factorized 4-input Bitonic SN only requires 2 CS operators instead of 6. However, the latency will be 6 instead of 3 and no other list can be inserted at the input during this calculation reducing the throughput of the architecture. It is worth to note that this solution requires also 8 Multiplexers in addition.

For evaluating the required resources and the execution time for a generic *M*-input SN with a factorization level *L* (*M* and *L* are power of two) some general equations have been derived. The number of stages and the number of CS operators for Bitonic and Even-Odd SN are:

$$\begin{aligned}
C_{Bitonic}(M,L) &= \frac{M}{L} 2^{s-1} + \left(\frac{p^2+p}{2} - \frac{s^2+s}{2} \right) 2^{p-1} \\
C_{Even-Odd}(M,L) &= \frac{M}{L} 2^{s-1} + \left[(p^2 - p + 4) 2^{p-2} - 1 \right] - \frac{M}{L} \left[(s^2 - 2 + 4) 2^{s-2} - 1 \right] \\
S_{Bitonic}(M) &= S_{Even-Odd}(M) = S(M) = \frac{p^2+p}{2}
\end{aligned} \tag{2}$$

where p and s are $\log_2(M)$ and $\log_2(L)$, respectively. It is worth to note that if *L=2*, the fully pipelined synchronous SN without factorization is achieved. As said above, when the factorization is adopted some multiplexers must be added. The number of multiplexers can be calculated as in (3).

$$\begin{aligned}
Mux_V(M,L) &= \frac{M}{L} 2^s \\
Mux_P(M,L) &= \frac{M}{L} 2^s
\end{aligned} \tag{3}$$

where Mux_V and Mux_P are the number of multiplexers for the capacitor voltages and for the position values, respectively. The number of inputs of these multiplexers is:

$$Mux_{inp}(L) = \frac{s^2 + s}{2} \tag{4}$$

The number of Flip-Flops (FFs) can be expressed as:

$$FF(M,L) = (b_v + b_p)(p^2 + p)2^{p-1} - \frac{M}{L}(b_v + b_p)(s^2 + s)2^{s-1} + \frac{M}{L}(b_v + b_p)2^{s+1} \tag{5}$$

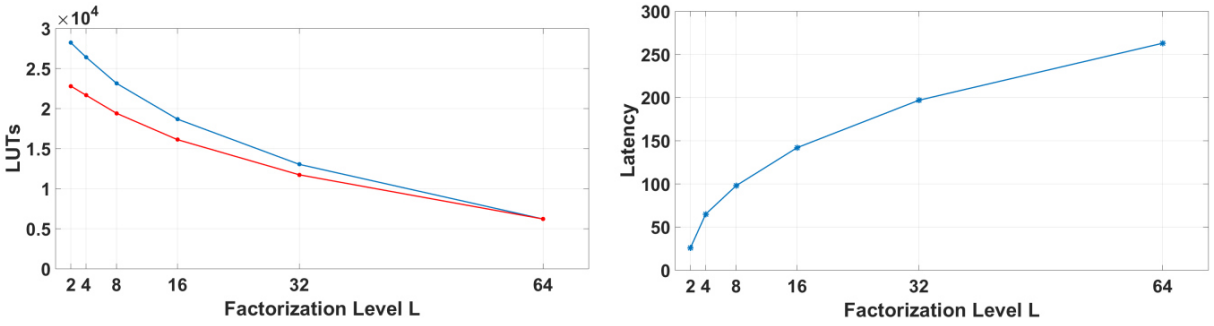
By assuming that each FF is placed in the same slice of either the CS operator or the multiplexer, the total number of LUTs is resulted by:

$$LUT(M,L) = \frac{5}{2}b_v C(M,L) + 2C(M,L)b_p + round\left(\frac{Mux_{inp} + \log_2(Mux_{inp})}{LUT_{inp}}(b_v + b_p)Mux_V + 0.5\right) \tag{6}$$

where LUT_{inp} is the number of LUT inputs (it depends to the FPGA family). The execution time for sorting 6 lists with an M-input SN with factorization level L is expressed in (7). It is worth to note that it is the same for both the Bitonic and the Even-Odd SN but two cases must be distinguished: L equal to 2 and L larger than 2.

$$\begin{aligned} t_{ex}(M,L) &= \left(\frac{p^2 + p}{2} + 1\right)t_{clk} + 5t_{clk} && \text{for } L = 2 \\ t_{ex}(M,L) &= \left(\frac{p^2 + p}{2} + \frac{s^2 + s}{2} + 1\right)t_{clk} + 10\left(\frac{s^2 + s}{2} + 1\right)t_{clk} && \text{for } L > 2 \end{aligned} \tag{7}$$

Fig. 7(a) shows the LUT number for a 64-input fully pipelined synchronized SN with different factorization level. The corresponding latency (number of clock cycle required for achieving the result) is shown in Fig. 7(b). The figures have been obtained assuming $b_v = 12$ and $b_p = 6$. As expected, increasing the factorization level the required number of LUTs decreases but the latency increases. With the maximum factorization level almost 6200 LUTs and 260 clock cycles are required for sorting the SMs of 6 arms. The execution time can be easily obtained by multiplying the latency number with the clock period. As an example, supposing a clock frequency equal to 100 MHz, the execution time will be 2,6 µs which is quite low in comparison with the sampling period usually used in MMC applications (10 ÷ 100 µs).



(a) (b)

Fig. 7: (a) LUTs Evaluation Bitonic (blue line) vs Even-Odd (red line); (b) Latency Evaluation (the same for both).

FPGA Implementation and Validation of the Bitonic SN

The implementation of the Bitonic SN with the maximum factorization level and different input length is now afforded. The Vivado Design Suite from Xilinx has been used during the implementation process and the Vivado Simulator has been adopted for validating the developed Bitonic SN module. This module consists of a state machine for ensuring the synchronism and a data path, as shown in Fig. 8. The data path is composed of several CS operators, depending on the number

of inputs, and a *Map* module that properly feed the CS outputs back to the input; with other words it implements the multiplexers shown in Fig. 6(b). The inputs of the Bitonic SN module are the capacitor voltages, the clock and the start signal. The SM positions, sorted according to their voltages, and the *done* signal are the outputs.

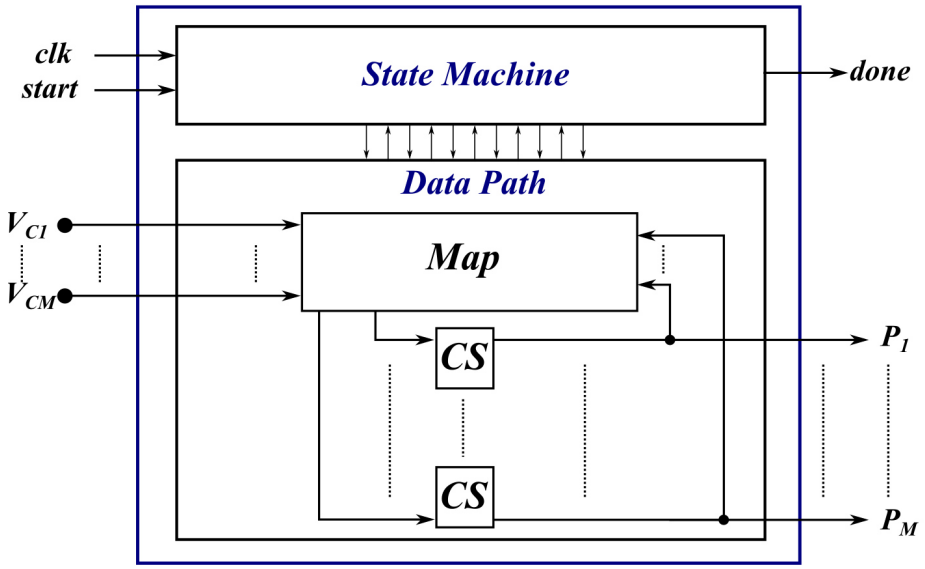


Fig. 8: Bitonic SN FPGA-implementation with the maximum factorization level.

Four Bitonic SN with different input number (8, 16, 32, 64) have been implemented. The corresponding required resources are very close to the one evaluated in the previous section, as shown in Fig. 9. Actually, a small difference appears with *M=64*, this could be due to the optimization tool of the Vivado Design Suite.

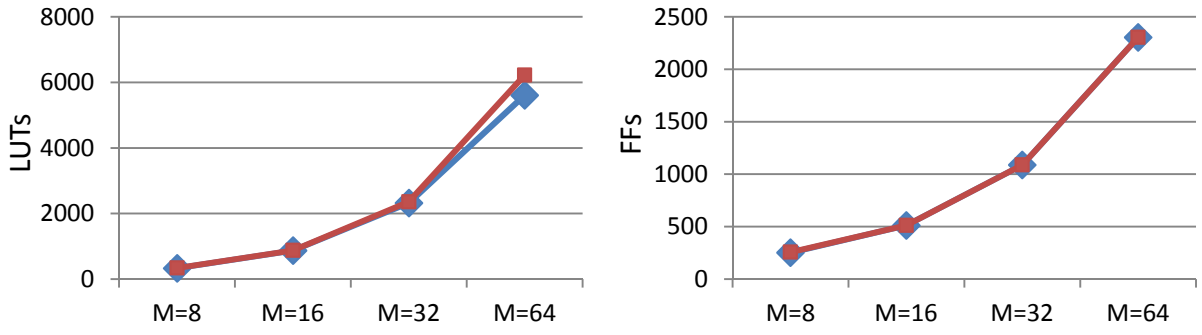


Fig. 9: Comparison between the required resources (blue line) and the one evaluated as previously shown (red line).

Considering a Xilinx Spartan VI XC6SLX45 FPGA and the Bitonic SN with highest factorization level and 64 inputs, the corresponding required resources are 21 % of the available ones.

The Vivado Simulator has been used for validating the proposed FPGA SN implementation. The result of the 8-input Bitonic SN module for one generic arm is shown in Fig. 10. On the left, the unsorted SM capacitor voltages V_{Ci} are shown along with their physical position P_i. The timing behavior of the SN is depicted and the correct sorted capacitor voltage list, in addition to the SM positions, is achieved after *18* clock cycles.

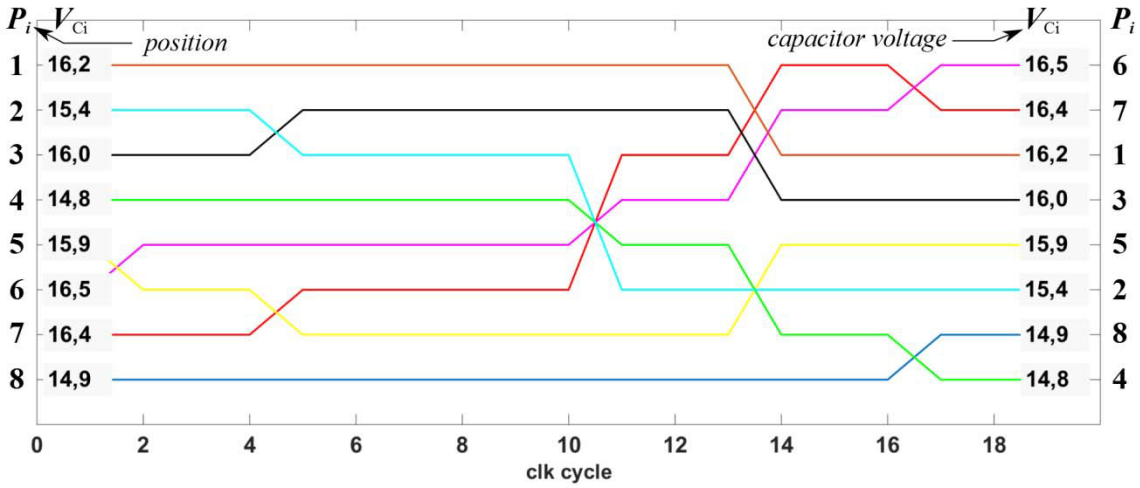


Fig. 10: Sorting example of a 8-input Bitonic SN with the maximum factorization level.

Conclusion

In this paper sorting networks have been proposed for hardware implementation in MMC applications. The main advantages of these SNs are their fixed parallel structure and the fact that they do not require iterative or branches instructions. Basically, two SNs have been considered: the Bitonic SN and the Even-Odd SN due to their attractive modular aspect and the low requirement of CS operators. However, the necessary resources quickly increase to the growth of the number of inputs. Then, in order to save FPGA resources, the SN architecture has been factorized. Different factorization levels, for both the SNs, have been compared in terms of required LUTs and latency. The execution time can be easily calculated and it has been shown that it is lower than the sampling period usually used in MMC application. A comparison between the pre-evaluated number of LUTS/flip-flops and the required ones has also been given in the paper. The proposed solution is flexible and it allows reaching a compromise between the execution time and the required resources.

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New MMC Capacitor Voltage Balancing using Sorting-less Strategy in Nearest Level Control

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***Abstract*— This paper proposes a new strategy for balancing the Capacitor Voltages (CVs) for Modular Multilevel Converters (MMCs). The balancing is one of the main challenges in MMC applications and it is usually solved by adopting a global arm control approach. For performing such an approach, a sorted list of the SubModules (SMs) according to their capacitor voltages is required. A common way to accomplish this task is to implement a sorting algorithm in the same controller used for the modulation technique. However, the execution time and the computational efforts of these kinds of algorithms increase very rapidly when the number of SMs grows. A novel idea is presented in this paper by using a mapping strategy that directly stores in a ranked list the SMs according to the measured CVs. Avoiding the use of sorting algorithms leads to a considerable reduction of the execution time as well as the computational efforts.**

Keywords—Modular Multilevel Converters; Converter Control; Field Programmable Gate Array (FPGA); Capacitor Voltage Balancing (CVB)

I. INTRODUCTION

The Modular Multilevel Converter (MMC) shows several advantages, such as scalability, high modularity, low switching losses, low Total Harmonic Distortion (THD) and high reliability. Thanks to these benefits, this topology has become a promising solution in several applications, like in High Voltage Direct Current (HVDC), STATic COMpensators (STATCOM) and in high-power motor drivers. However, this new technology also presents different challenges, for instance the need to control the circulating current, ensure the balance of the losses and energy distribution among the Sub-Modules (SMs) [*1*] [*2*]. Concerning the gate pulse generation, different algorithms are commonly adopted, such as the Phase-Shifted Pulse-Width Modulation (PS-PWM) or the Nearest Level Control (NLC). For both cases a proper Capacitor Voltages Balancing (CVB) algorithm is needed to be inbuilt in the modulator in order to maintain the CV balanced and then ensure a stable MMC operation.

Mainly, two kind of CVB control algorithms can be found in literature: the individual control approach (used independently in each SM applied for PS-PWM) [*3*] and the global arm control approach (used in NLC) [*2*]. On one hand, the individual control approach is based on a closed loop control. The aim is to maintain the capacitor voltage closes to a global reference value given by the central control unit. For this purpose, different references are obtained for the pulse generation by adjusting the modulation signal of each Sub-Module (SM). In this case, the main challenge is the choice of the control parameters. Unsuitable parameters could affect the other control loops or, in the worst case, leads to the instability. On the other hand, the global arm control approach consists in selecting the suitable SMs for insertion or bypass, according to the capacitor voltage and the arm current direction. In this approach, no control loop is needed but a sorting, based on the capacitor voltages, is mandatory.

The balancing control for NLC is usually made by using the so-called Sorting Algorithms (SAs). They sort the SMs by comparing and swapping the capacitor voltages. Several sorting techniques are presented in the technical literature, for instance: bubble sorting and odd-even method [*4*]. However, these algorithms always have the same problem: the execution time and the computational efforts increase very rapidly when the number of SMs grows. In order to overcome this problem several authors have proposed max/min methods for finding only the SMs with the maximum and the minimum capacitor voltage [*5*] [*6*]. Nevertheless, when more capacitors are close to the maximum allowable voltage, or when faults appear on the system, more SMs are needed to be inserted or bypassed in the same sampling period. Thus, the system has to be prepared for the worst case scenario. Running multiple times the max-min method could be a solution, but this choice also leads to the aforementioned problem: the controller response becomes slow.

For these reasons, a new Capacitor Voltage Mapping Strategy (CVMS) that directly creates a sorted list based on the CV of the SMs is proposed in this paper. This leads a significant reduction of the CVB execution time in comparison with the one obtained by using the SAs. Moreover, it does not require any iterative or branch instructions and the computational efforts remain limited. All these advantages are achieved at the cost of a slight increase of the required memory, which is present in high quantity in the modern microprocessors, Digital Signal Processors (DSPs) or Field Programmable Gate Array (FPGA) devices.

The paper is divided as follows: firstly, the MMC is presented and the classical flowchart used in NLC is displayed. After that, the proposed technique is described. Then, a comparison with the common used bubble sorting

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algorithm, in terms of required memory and execution time, is made. Afterwards, different simulations are performed to demonstrate the effectiveness of the proposed strategy. Finally, the conclusions are drawn.

II. Modular Multilevel Converter

Fig. 1 presents a general schematic representation of a three phase grid connected MMC. Each phase consists of an upper and a lower arm which in turn is composed by series connected arm inductor L_{arm}, the parasitic resistances present in the arm R_{arm} and the SMs [7]. One of the most often used configurations for SMs is the half-bridge, which consists of two switches (typically IGBTs or MOSFETs) with two antiparallel diodes and a capacitor C, as shown in Fig. 1. The SM can take two operating states, which results in: inserted or bypassed capacitor in the arm circuit.

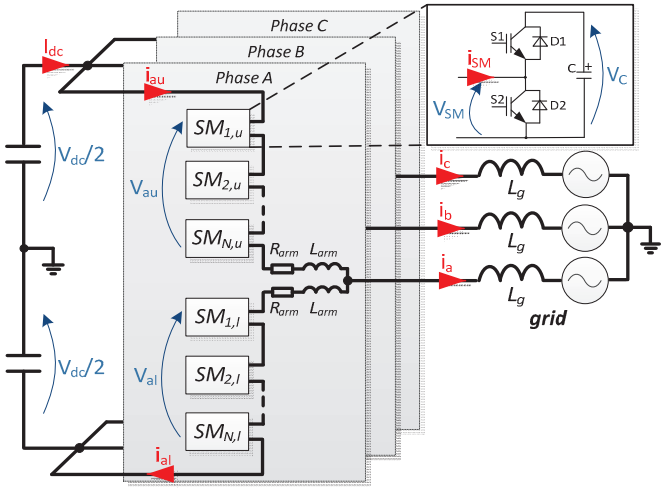

Fig. 1: Schematic representation of a three phase grid connected MMC.

At each sampling time the number of SMs to be inserted is chosen by the modulation technique. One of the most common modulation techniques is the NLC method [8]. The block diagram of a three-phase MMC controller for the phase "a" based on such a technique is depicted in Fig. 2. The phase reference voltage V_{ref} is resulted by the outer current control loop from the measured grid currents and voltages, and adjusted in according with the circulating current control and the averaging control, as described in [3]. The insertion indices n_u and n_l are then calculated for the upper and lower arm, respectively, using the NLC as expressed in:

$$n_{pm} = round\left(\frac{V_{ref_{pm}}}{V_{dc}}\right) \quad (1)$$

Where the indices p and m represent the phase ($p = a, b, c$) and the arm ($m = u, l$), respectively. From the NLC point of view it is indifferent which SMs are inserted, but it is important the overall number of the inserted/bypassed SMs to be fulfilled. This freedom is used by the CVB control algorithm for ensuring the balance between the capacitor voltages in the arm [5].

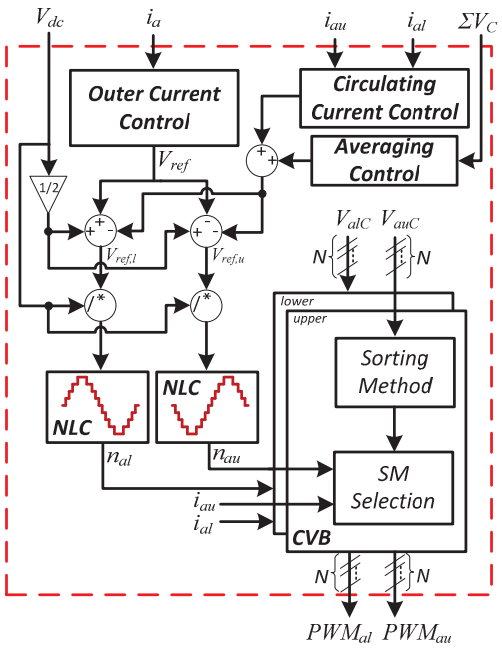

Fig. 2: Block Diagram of the grid connected MMC controller for the phase a.

The basic elements of the CVB control algorithm are the sorting and selection techniques. The sorting method sorts the SMs according to the measured capacitor voltages V_{pmCi}. On the other hand, the selection technique selects the SMs to be inserted based on the direction of the arm current i_{pm} and on the sorted SM list. The best performance of the CVB control algorithm is achieved when it is executed in each sampling period, as shown in Fig. 3. However, this requires a relatively high number of switching and in literature several methods to reduce it can be found [8] [9] [10]. The focus of this paper is to prevent the sorting, by presenting a new capacitor voltage mapping strategy that can directly create a sorted list for the CVB control algorithm.

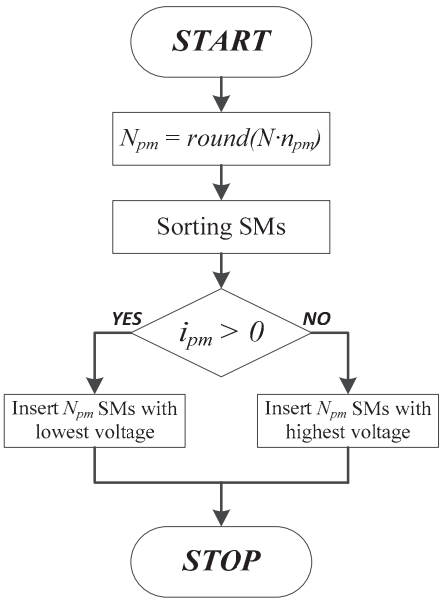

Fig. 3: Flowchart of the basic capacitor voltage balancing algorithm in NLC.

III. Proposed Capacitor Voltage Mapping Strategy

The proposed strategy consists in mapping the SMs in a memory based on their capacitor voltages, achieving in this way a sorted list right after the ADC is performed. In normal operation, the SM capacitor voltages vary between a minimum and a maximum value, $V_{c_{min}}$ and $V_{c_{max}}$, respectively. These limit quantities are the design parameters of the MMC. Based on these limits the size of capacitor is chosen, then the capacitor voltage ripple can be calculated as presented [*11*]. This range can be divided into different sub-ranges with an amplitude equal to ΔV:

$$\Delta V = \frac{V_{c_{max}} - V_{c_{min}}}{M} \tag{2}$$

where M is the number of sub-ranges. Each sub-range corresponds to a specific memory location as shown in the concept scheme in Fig. 4. For example all the SM with capacitor voltages in the range $\left[V_{c_{min}} : V_{c_{min}} + \Delta V\right]$ will be mapped in the position 0 of the memory; all the SM with capacitor voltages in the range $\left[V_{c_{min}} + \Delta V : V_{c_{min}} + 2\Delta V\right]$ in the position 1; and so on.

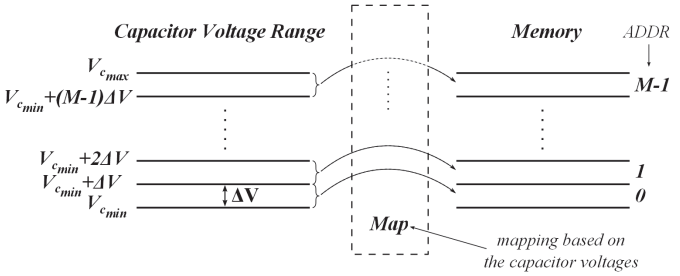

Fig. 4: Concept of capacitor voltage range mapping in the memory.

To each sub-range corresponds a memory address $ADDR_i$ obtained by scaling the capacitor voltage V_{c_i}. This scale operation consists in a subtraction, a multiplication and a rounding operation, as shown in Fig. 5. In order to be able to select the proper SM, a position number (named here P_{Ci}) is assigned for each SM based on the physical placement of the SMs in the arm. The position number is then stored in the memory according to the mapping of the measured capacitor voltage explained above.

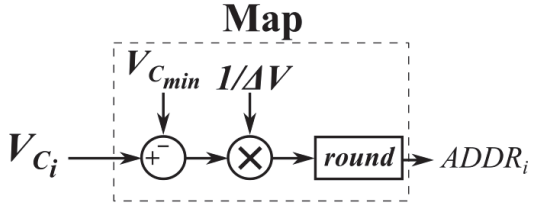

Fig. 5: Block Diagram of the proposed CVMP. The memory address is evaluated from V_{Ci} and P_{Ci} is stored in the memory.

Due to the approximately equal distribution of the capacitor voltages between the SMs, more SMs can have close voltage levels which fall in the same range. For this reason each sub-range, and then each address, has to correspond to a First-In-First-Out (FIFO) memory, as shown in Fig. 6. P_{Ci} is then stored in the cell $c_{ADDR,k}$ according to the evaluated address $ADDR_i$ and the status of the FIFO memory k (i.e. how many positions are already stored in that FIFO). With other words, the FIFO memory array can be seen as a matrix where the row is selected in accordance with the evaluated $ADDR_i$ and the column is decided according to the status of the FIFO memory. In order to avoid overflow in the FIFOs the depth should be equal to the number of SMs N. However, it can be reduced to N/2 by considering the fact that when half capacitors have high voltages the other half should necessarily have low voltages in order to fulfill: $\sum_{i=1}^{N} V_{Ci} = V_{dc}$. In case the capacitors have similar voltages, instead, they fall in the same FIFO memory, and then the balancing is working well and no interaction is needed. Nevertheless, a reduction of the required memory can be obtained as mentioned above, in this work, the depth of the FIFO memory is chosen equal to the number of SMs N. The number of FIFO memories, instead, is equal to the number of sub-ranges (noted with M) and the size of each memory cell $c_{ADDR,k}$ is equal to the bit-length of the SM position P_{Ci}.

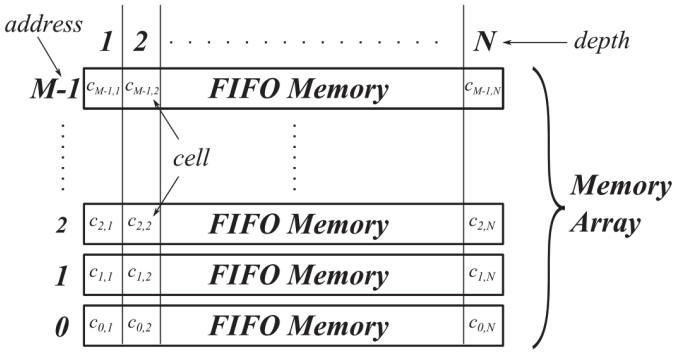

Fig. 6: Memory Array: it consists of M FIFO memories with depth equal to N. The i-capacitor position P_{Ci} is stored in the cell $c_{ADDR,k}$ where the ADDR is evaluated from the V_{ci} and k depends to the FIFO memory status.

After having stored all the SM positions in the memory array, the SMs which need to be inserted or bypassed are obtained by reading the memory from the top to the bottom or from the bottom to the top according to the arm current, as it is shown in the flowchart from Fig. 3. When a FIFO memory string is empty, the string located at the next address must be read. Therefore, the SM positions are sorted according to the SM capacitor voltages directly after the digital CV values are read from the ADC avoiding the use of sorting algorithms.

For example, by considering an MMC with *N=6*, and with a $V_{c_{min}} = 14\,V$, $V_{c_{max}} = 18\,V$ and a sub-range of *M=8*, resulting $\Delta V = 0.5\,V$, the mapping can be done as presented in Fig. 7. In TABLE 1 the results of each operation are reported, where it is shown in which way the memory addresses are obtained based on each SM's voltage. It is easy to see that the SM positions are ordered according to their capacitor voltages. Indeed, for instance, the SM with the lowest capacitor voltage (SM with position 3) is correctly placed in the FIFO memory with address 1.

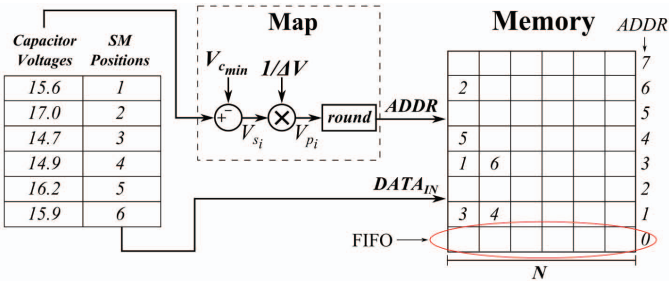

Fig. 7: Mapping of the SM positions in the memory in the presented example ($N = 4$, $V_{c_{min}} = 14\,V$, $V_{c_{max}} = 18\,V$ and $M = 8$).

On the other hand, the SM with the largest capacitor voltage (SM with position 2) is placed at the address 6. It is important to notice here that the measured voltage level is not stored in the memory, only the physical position of the SM. This is possible due to the fact the NLC control algorithm does not need the individual capacitor voltage value. Only the sum of the capacitor voltages from the arm is used for the averaging control, as shown in Fig. 2.

TABLE 1: Results of each operation of the previous example.

P_{c_i}	V_{c_i}	V_{s_i}	V_{p_i}	$ADDR_i$
1	15.6	1.6	3.2	3
2	17.0	3.0	6.0	6
3	14.7	0.7	1.4	1
4	14.9	0.9	1.8	1
5	16.2	2.2	4.4	4
6	15.9	1.9	3.8	3

The accuracy of the mapping depends on the amplitude of the sub-ranges ΔV and then on the amount of the used memory. From capacitor voltage balance point of view, it is not important the small deviation between the capacitor voltages, rather the high capacitor voltages which can exceed the safety limit of the SM. Switching optimized NLC methods, such as tolerance band capacitor voltage control [*8*], allows similarly a band inside which the capacitor voltages can freely vary, performing extra switching only when the band is exceeded. Then, a good compromise can be reached for guaranteeing the right behavior of the CVB algorithm and avoiding a significant memory usage. An M comprises between 16 and 64 can achieve this goal, as it is resulted later in the simulation. On the other hand, the advantages of the proposed method are to drastically reduce the execution time and the computational efforts for sorting the SMs, as also demonstrated in the next section.

IV. Memory and Execution Time Evaluation

In this section a comparison in terms of required memory and execution time is made between the classical bubble sorting algorithm and the proposed mapping strategy.

Regarding the total required memory, the needed size in bytes ($\text{size}_{\text{CVMS}}$) of the proposed CVMS depends on the number of levels M, the depth of the FIFO memories (so on the number of modules N) and on the number of bits for the SM position $log2(N)$ as expressed in (3).

$$size_{CVMS} = \frac{M \cdot N \cdot log2(N)}{8} \tag{3}$$

On the other hand, the required memory for the bubble SA is based on the number of SMs N and on the ADC resolution of the capacitor voltage (noted with b_V). Then the size of the bubble SA can be expressed as:

$$size_{BSA} = \frac{N \cdot b_V + N \cdot log2(N)}{8} \tag{4}$$

Fig. 8 (a) and Fig. 8 (b) show the size of the memory space required for a bubble SA (the blue line, that obviously does not depend on M) and the proposed procedure (the red line) when the bit number of the capacitor voltages is 12 and the number of SMs per arm is 8 and 64, respectively. It is worth to note that this comparison is valid for all sorting algorithms because in all the cases at least the capacitor voltages and the SM positions have to be stored.

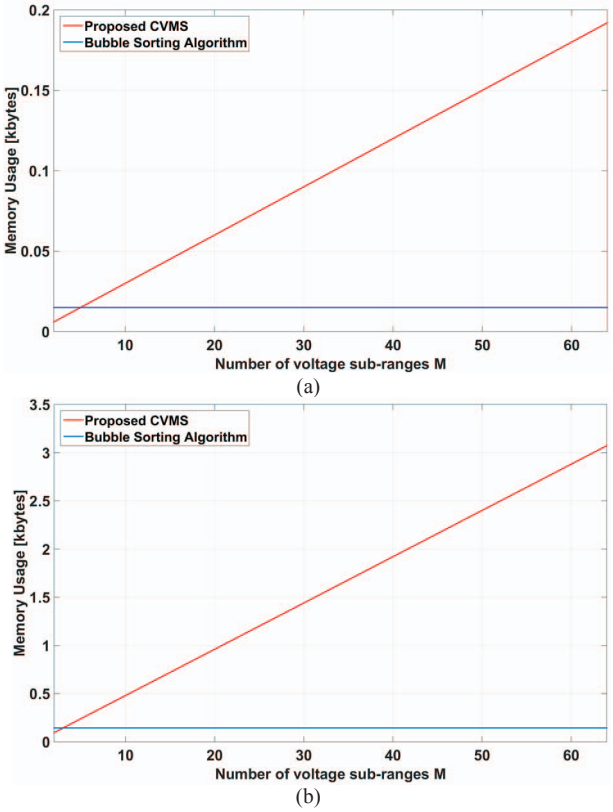

Fig. 8: Evaluated memory usage for the bubble SA and the proposed CVMS with different number of sub-ranges M: (a) N = 8; (b) N = 64.

Therefore, in case of 64 SMs and M equal to 64, the bytes memory usage for the bubble SA and for the proposed method is 0.14 and 3 kbytes, respectively. However, in the modern digital platforms a memory of several kilobytes is not an issue. Indeed, microcontrollers or FPGA platforms are equipped with more and more memory for almost the same price. For instance, considering the TI microcontroller TMS4320F28335, which might be a proper choice for

controlling this kind of converter [*12*], is equipped with 68 kbytes of memory. Regarding to FPGA platforms, possible solutions, in MMC applications, can be either the Xilinx Virtex-7 FPGA board [*5*] or the Xilinx Zynq System on Chip platform [*13*]. Both provide a large amount of block RAM (at least 240 kbytes). Then, the proposed CVMS requires less than 5% of the available memory for these devices.

Along with the memory, the used resources should be also considered; the proposed mapping strategy requires: a multiplier, a subtractor and a rounding operator. On the other hand, when bubble SAs are implemented in a microcontroller or in a DSP, iterative instructions (performed with while/for loop) are needed to perform the compare operations. This leads to an increment of the CVB execution time. Another solution could be to implement these kinds of algorithms in a FPGA for exploiting the inherent parallelism of the algorithm. In this case, the required resources significantly increase [*5*].

A comparison in terms of execution time has been also performed. For this purpose, both methods are divided into different steps, as shown in TABLE 2, and the corresponding execution time is evaluated. Regarding to the Bubble SA, it firstly requires storing the V_{Ci} and the P_{Ci} in the memory for which at least N clock cycles are required. After the reading procedure is finished, the sorting of the list can be started. The time for accomplishing this task clearly depends on the number of SMs N but also on the values of CVs, i.e. how much the list is unsorted. By considering that the CVs do not significantly change in one sampling period, a reduction of the execution time can be achieved. Indeed, after having updated the CV value, a pre-sorted list is obtained if the previous sorted list order is kept. However, in case of faults, the controller should be able to face with a possible totally unsorted list. Then, the worst case has to be always taken into account during this evaluation. Eventually, the required SMs *n* have to be read from the memory by requiring at least *n* clock cycles. On the other hand, the CVMS directly stores the SM positions in the right order by performing the storing and the sorting in the same step, as shown in TABLE 2. Finally, the required SMs can be read from the memory. In this case, the execution time can be bigger than the one obtained with the Bubble SA because in the case a FIFO memory is empty the SMs have to be selected from the FIFO memory located at the next address.

TABLE 2: Main steps of the Bubble SA and the proposed CVMS with the corresponding evaluated execution time.

Bubble Sorting Algorithm	***Proposed CVMS***
1) Store the V_{c_i} and the P_{c_i} in the memory: $t_1 \simeq N\, t_{clk}$	1) Store the P_{c_i} as explained before: $t_1 \simeq 3N\, t_{clk}$
2) Sort the list (worst case) [4]: $t_2 \simeq 5\left[(N+1)\frac{N}{2}\right] t_{clk}$	
3) Read from the memory: $t_3 \simeq n\, t_{clk}$	2) Read from the memory (worst case): $t_2 \simeq N\, t_{clk}$

For instance by taking an example with N=64 and a clock cycle of the controller equal to 20 ns, the execution times of the bubble SA and the proposed procedure would result in almost 210 µs and 5.12 µs, respectively, which is a reduction of app. 40 times. In Fig. 9 the two methods are compared with different value of N. The execution time of the bubble SA exponentially increases in function to the number of SMs, which highlights the improvement obtained by using the proposed method.

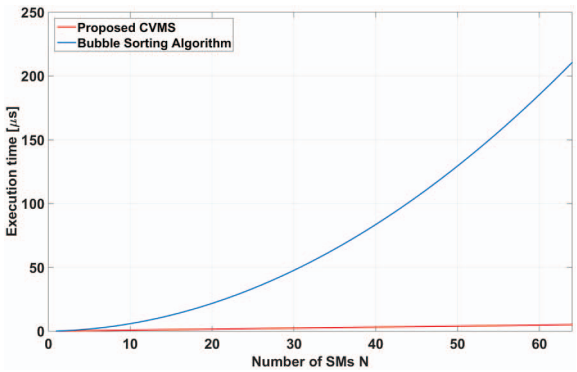

Fig. 9: Comparison of the evaluated execution time at different N for the bubble SA and the proposed CVMS.

V. Simulation Results

In order to validate the proposed CVMS several simulations have been performed in PLECS® power electronic simulation tool. In TABLE 3 the parameters of the MMC built in the simulation platform are given.

TABLE 3: MMC Parameters

DC-link Voltage V_{DC}	200 kV
SM Capacitor C	36 µF
Arm Inductance L_{arm}	50 mH
Arm Resistance R_{arm}	1 Ω
Number of SM N	16
Sampling frequency f_s	10 kHz

The MMC is connected to the grid whose parameters are displayed in TABLE 4.

TABLE 4: Grid Parameters

Grid frequency f_{grid}	50 Hz
Grid Voltage V_{grid}	121.2 kV
Grid Inductance L_{grid}	16.7 mH
Grid Resistance R_{grid}	0.52 Ω

The proposed mapping strategy for the CVB is implemented in a C-script in PLECS® with different number of FIFO memories M. V_{Cmin} and V_{Cmax} are equal to 10 kV and 35 kV, respectively. Moreover, all the voltages lower than V_{Cmin} are mapped in the first position of the memory and all the voltages bigger than V_{Cmax} in the last position. The resulting capacitor voltages are compared with the one obtained by using the bubble sorting algorithm, as shown in Fig. 10. It can be noticed that the capacitor voltage balancing

capability of the proposed CVMS tends towards the one obtained with the bubble SA when M increases.

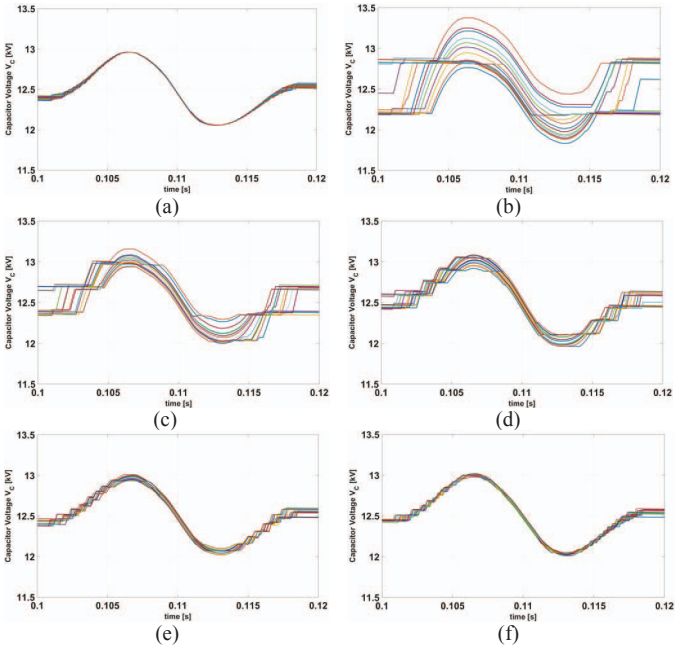

Fig. 10: Steady-state capacitor voltages: (a) bubble sorting algoritm; (b) CVMS with M = 8; (c) M = 16; (d) M = 32; (e) M = 64; (f) M = 128.

In order to appreciate the improvement obtained by increasing the number of FIFO memories the Root Mean Square Deviation (RMSD) of the capacitor voltages are calculated for each arm as in (5). RMSD measures the deviation of the CVs from their average in a sampling instant k.

$$RMSD_{pm}(k) = \sqrt{\frac{\sum_{i=1}^{N}\left(V_{C,pmi}(k) - V_{av,pm}(k)\right)^2}{N}} \qquad (5)$$

where $V_{C,pmi}(k)$ and $V_{av,pm}(k)$ are the i-capacitor voltage in the p-phase of the m-arm (upper or lower) and the average of the capacitor voltages for the same arm and in the same sampling instant, respectively. An average of the RMSD in a period of 0.5 seconds is made for achieving a conglomerated indicator, as shown in TABLE 5. The results of the mapping strategy tend to the ones obtained by the bubble sorting algorithm by increasing M.

TABLE 5: Averaged RMSD of the capacitor voltages for the bubble SA and the proposed CVMS with different M.

Bubble Sorting Algorithm	115.06 V
CVMS with M = 8	323.80 V
CVMS with M = 16	212.75 V
CVMS with M = 32	160.28 V
CVMS with M = 64	136.68 V
CVMS with M = 128	125.18 V

In order to show the dynamic response of the proposed CVMS, the initial capacitor voltages were chosen to have a random distribution and several simulations are performed with different M, as depicted in Fig. 11.

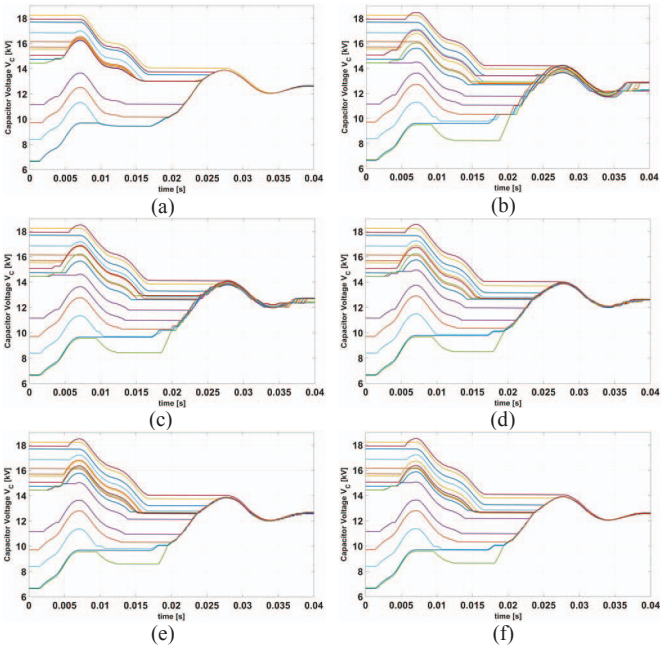

Fig. 11: Transient capacitor voltages: (a) bubble sorting algoritm; (b) CVMS with M = 8; (c) M = 16; (d) M = 32; (e) M = 64; (f) M = 128.

In this case the RMSD is calculated during the transient and the results for each sampling period are shown in Fig. 12. It is possible to see that the CVMS has a response time almost equal to the one obtained with the bubble sorting algorithm, for each M.

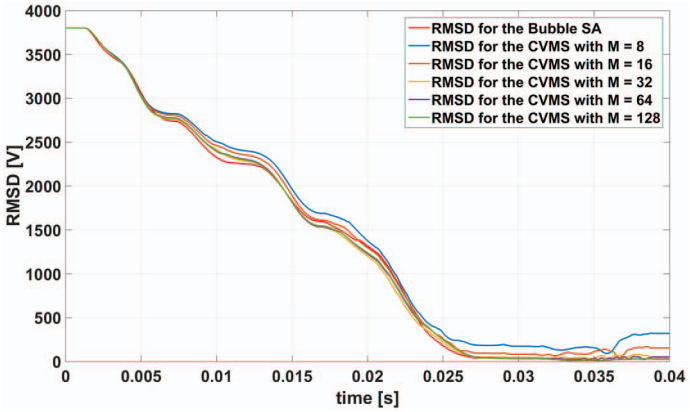

Fig. 12: RMSD during capacitor voltage transient for bubble sorting algorithm and CVMS with M = 8, 16, 32, 64, 128.

Then, the main difference between the bubble SA and the proposed CVMS is in the steady-state operation where the level of the unbalance increases when M is small. This larger deviation from the ideal capacitor voltage value could also affect the rounding operation of the NLC influencing the output current. Therefore, in order to demonstrate the effectiveness of the presented strategy, the circulating current and the output current of the phase "a" for each case are shown in Fig. 13 and Fig. 14, respectively.

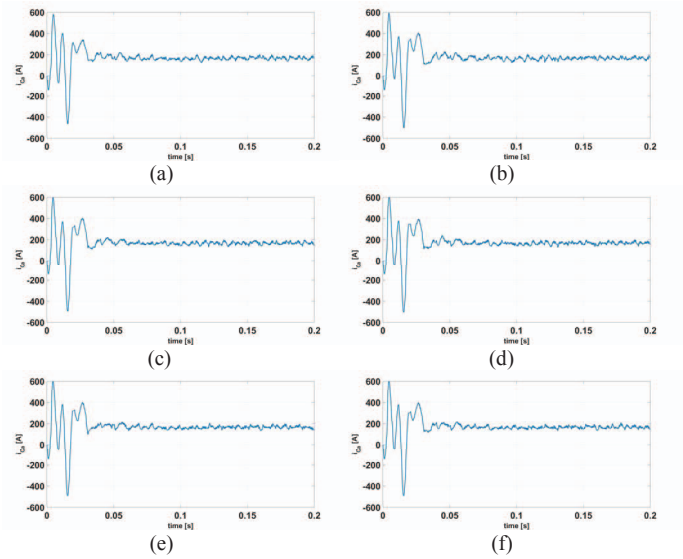

Fig. 13: Circulating current of the phase "a": (a) bubble sorting algoritm; (b) CVMS with M = 8; (c) M = 16; (d) M = 32; (e) M = 64; (f) M = 128.

Based on the simulation results the proposed technique has minimal influence on the circulating and output currents independently on the value of M. TABLE 6 shows the evaluated THD of the output voltage for each case and it is evident that the influence of the proposed mapping strategy is again negligible. This could be due to the fact that the actual number of SMs is quite high (N = 16) by reducing the effect of the unbalancing of the CVs. For this reason, another simulation with N=4 is performed and the evaluated THDs are presented in TABLE 7.

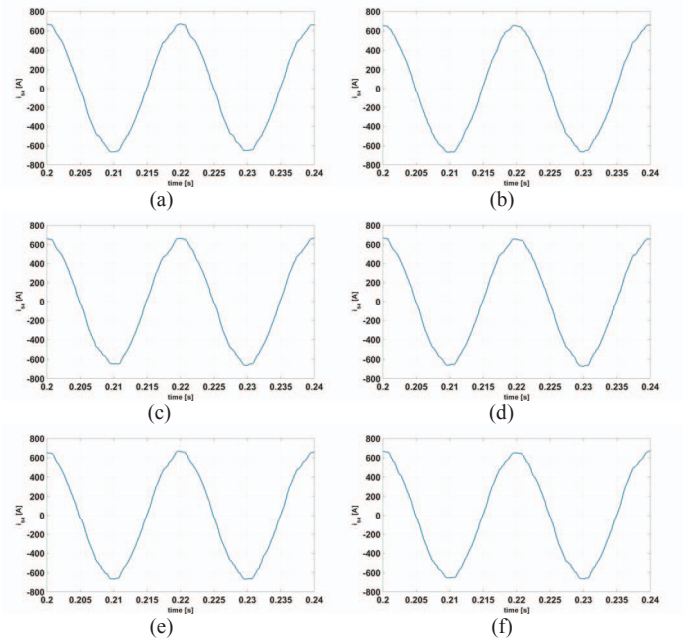

Fig. 14: Output current of the phase "a": (a) bubble sorting algoritm; (b) CVMS with M = 8; (c) M = 16; (d) M = 32; (e) M = 64; (f) M = 128.

TABLE 6: THD evaluation for the output voltage of phase "a" when N = 16.

Bubble Sorting Algorithm	1.21 %
CVMS with M = 8	1.17 %
CVMS with M = 16	1.24 %
CVMS with M = 32	1.21 %
CVMS with M = 64	1.21 %
CVMS with M = 128	1.23 %

It is evident that also by reducing the number of SMs the THD of the proposed method is close to the one obtained with the bubble sorting algorithm. Therefore, the mapping strategy does not have any effect on the voltage THD.

TABLE 7: THD evaluation for the output voltage of phase "a" when N = 4.

Bubble Sorting Algorithm	6.44 %
CVMS with M = 8	6.23 %
CVMS with M = 16	6.41 %
CVMS with M = 32	6.46 %
CVMS with M = 64	6.48 %
CVMS with M = 128	6.41 %

Finally, based on the performed simulations it can be concluded that the operation of the MMC is marginally affected by the proposed mapping algorithm, while the time needed to obtain a sorted list is reduced considerably.

VI. Conclusion

In this paper a new simple and fast strategy to obtain a sorted list of the SMs according their capacitor voltages has been presented. The technique is based on assigning the CVs to different sub-ranges that are mapped in a list of FIFO memories. Unlike the CVB control based on sorting algorithm, the proposed method stores and sorts the SMs during the read of the ADC values by leading a significant reduction of the execution time and of the computational efforts, especially in case of high number of SMs. The main drawback of the proposed method consists in the increase of the memory usage, which is usually not an issue for the modern digital platforms, which are equipped with more and more embedded memory. A comparison with the bubble sorting algorithm in terms of required memory and execution time has been carried out. The slight increase of the memory space comes with a significant reduction of the execution time. For an MMC with N=64 the calculation time has been reduced by 40 times at the expense of 3kbytes memory. Thus with the proposed method a higher sampling frequency can be guaranteed or the same controller can handle a larger number of SMs in the MMC. Several simulations have been performed in both steady-state and transient conditions, resulting in almost identical performance between the bubble SA and the proposed capacitor voltage mapping strategy, in terms of output voltage THD, amplitude of circulating current and deviation of the capacitor voltages from their nominal value.

ACKNOWLEDGMENT

The paper has been supported by the EUDP grant number 64014-0137.

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